FERRANTI
DATA CONVERTERS

INTRODUCTION

Monolithic Data Converters

This handbook describes the comprehensive Ferranti range of monolithic I.C. data converters, which offer cost-effective solutions to a wide variety of data conversion problems.

This range, which is constantly being improved and extended, currently offers a choice of 40 different versions, including low-cost converters, microprocessor compatible A to D and D to A converters, dual slope DVM logic subsystems and a single channel CODEC.

The introductory section of this handbook is intended as a guide to the fundamental principles of data conversion and as an aid to understanding the terms used in converter specifications, which will enable the user to choose the most appropriate device for a particular application. The second section contains product data on the full range of Ferranti data conversion I.Cs.

1. DIGITAL TO ANALOGUE CONVERTERS

A Digital to Analogue converter (DAC) is a device which converts a digital data input into a corresponding analogue output. This output usually takes the form of a voltage or current.

1.1 Ideal Output Characteristics

If a unipolar voltage output and normal binary input coding are assumed, then the ideal transfer function of a linear DAC may be written as:

$$V_{out} = V_{FS} (B_1.2^{-1} + B_2.2^{-2} + B_3.2^{-3} + \ldots + B_n.2^{-n})$$

where B_1 is the most significant bit input (MSB) and B_n is the least significant bit input (LSB). Bits 1 to n can each assume a value of '1' or '0'. The number of bit inputs a DAC possesses is known as the RESOLUTION of the converter.

The smallest increment of output voltage is that contributed by the LSB and is equal to $V_{FS}.2^{-n}$.

The terms 'MSB', 'LSB' etc., are frequently used interchangeably to describe either the digital input or the corresponding analogue output.

The maximum output from a DAC is known as full-scale output (V_{FSO}).

It occurs when all inputs are '1' and is equal to $V_{FS} \left(\dfrac{(2^n - 1)}{2^n} \right)$. For example the maximum output of a 3-bit DAC is $\frac{7}{8} V_{FS}$.

The transfer function graph of an ideal 3-bit DAC is shown in figure 1. For each of the 8 input codes there exists a discrete analogue output
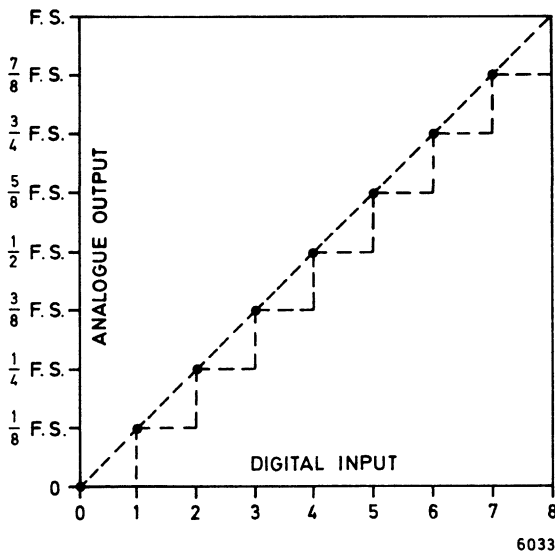

6033

Fig. 1. Transfer Characteristic of Ideal 3-bit DAC

1

D to A Converters

level, represented by a point on the graph. It should be emphasised that the transfer characteristic is not a continuous function and it is, therefore, not strictly correct to join the points with a continuous line, since this would imply that non-integral input codes and corresponding levels existed. However, a straight line is often drawn between zero and full scale to represent the 'ideal' transfer function on which all the points should lie.

Similarly, if the input code of a DAC is incremented using, say, a binary counter and clock generator, then the analogue output will be a staircase waveform. DAC transfer functions are frequently drawn as a staircase, since this is a convenient way of illustrating various errors that may occur in a DAC. However, such a graph is, strictly speaking, a plot of analogue output v. time rather than output v. input code.

1.2   Practical DAC Circuits

Figure 2 shows an example of a 3-bit DAC circuit based on a voltage-switching R-2R ladder network, a technique widely used in Ferranti converters.

Each 2R element is connected either to 0 volts or V_{FS} (V_{REF}) by transistor switches. Binary weighted voltages are produced at the output of the R-2R ladder, the value being proportional to the digital input number.
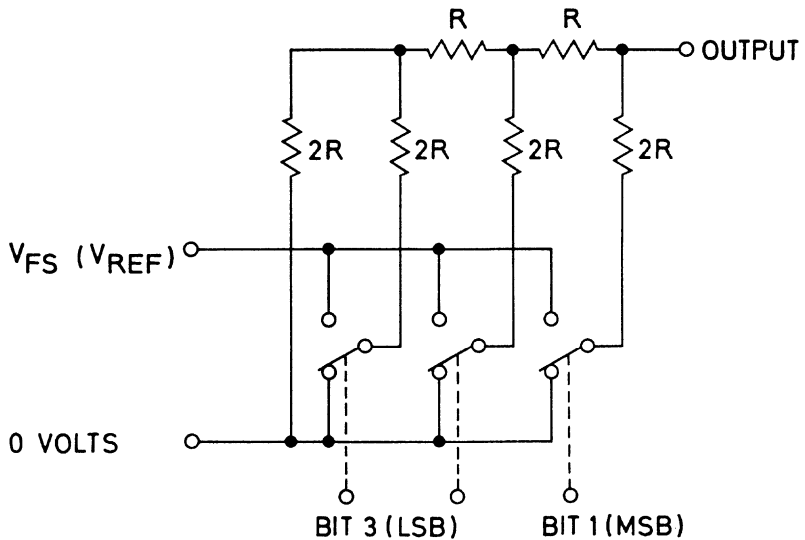

Fig. 2.   3-bit Voltage Switching DAC

D to A Converters

For example, it is fairly easy to see that if bit 1 is '1' and bits 2 and 3 are '0' then an output of $V_{FS}/2$ is produced. This is because the resistance of the ladder looking from the output through the first R is 2R, which forms a 2:1 attenuator with the 2R in series with the MSB switch. Output voltages for other input codes can similarly be calculated, and it can be seen that the ladder may be extended to any number of bits.

The voltage switching ladder technique is used in the ZN426, ZN428 and ZN429 series of D to A converters and also in the ZN425 dual-purpose A to D/D to A converter.

1.3 D to A Parameters and Definitions

1.3.1 Converter Errors

The ideal DAC assumes that all the resistors are perfectly matched and that the switches have zero resistance. In a practical converter this will not be the case and various errors will occur in the output.

1.3.2 Monotonicity

When the input code of a DAC is increased in 1 LSB steps the analogue output of the DAC should also increase, staircase fashion. If the output always increases in this manner then the DAC is said to be monotonic, i.e. the output is a single-valued function of the input. If, due to errors in the bit weighting, the output of the DAC decreases at any step, as shown in figure 3, then the DAC is said to be non-monotonic.
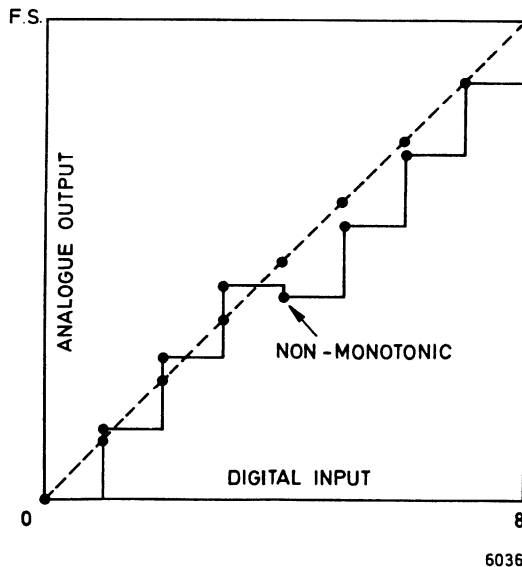
6036

Fig. 3. Non-monotonic DAC

3

D to A Converters

1.3.3 Offset (Zero Error)

Assuming unipolar operation and normal binary coding, when the input code is zero then the DAC output should also be zero. However, due to package lead resistances and offset voltages in the switches this will not be the case, and a small output offset may exist. This has the effect of shifting the transfer function so that it no longer passes through zero, as shown in figure 4.

1.3.4 Gain Error

If the reference voltage of a DAC is exactly the nominal value then the transfer characteristics of the converter should follow the ideal straight line. However, due to imperfections in the converter the transfer function may diverge from this line, as shown in figure 4. This error is known as gain error and is the difference between the slope of the actual transfer characteristic and the slope of the ideal transfer characteristic.
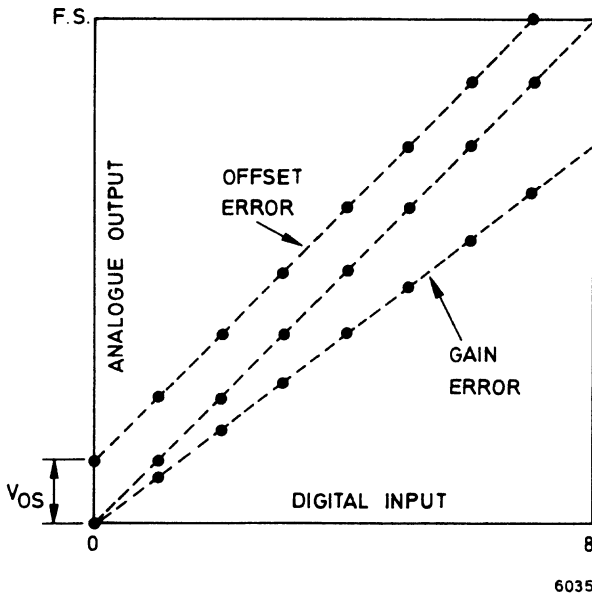

6035

Fig. 4. Illustrating Offset and Gain Errors

1.3.5 Linearity Errors

Offset and gain errors may be trimmed out so that the end points of the transfer characteristic lie at zero and V_{FSO}. However, even when this has been done, some or all of the intermediate points may not lie on the 'ideal' line. These errors, which cannot be trimmed out, are known as linearity errors.

4

1.3.6 Non-Linearity (Linearity Error)

This is the maximum amount, given either as a percentage of full scale or a fraction of an LSB, by which any point on the transfer characteristic deviates from the ideal straight line passing through zero and V_{FSO}. Non-linearity is illustrated in figure 5. A linearity error within the range $\pm\frac{1}{2}$ LSB assures monotonic operation. Note however that the converse is not true and a DAC may still be monotonic with large linearity errors, which is also shown by figure 5.

1.3.7 Differential Non-linearity

This is the maximum difference, specified as a fraction of an LSB, between the actual and ideal size of any one LSB analogue increment. This can be seen as an error in the step height of a DAC staircase. A positive value of differential non-linearity means that the step height is larger than nominal, whilst a negative value means that it is smaller than nominal. If it is more negative than –1 LSB then the DAC is non-monotonic. However, positive differential non-linearity may assume any value and a DAC can still be monotonic, as shown in figure 5.
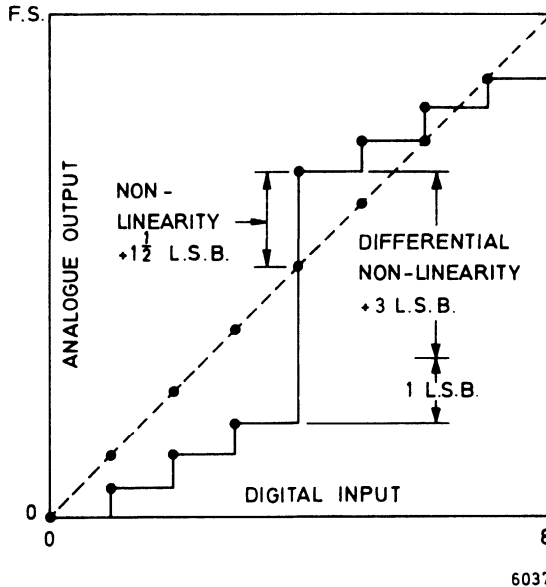

6037

Fig. 5. Illustrating Linearity Errors

5

D to A Converters

1.3.8 Resolution

As stated earlier, the resolution of a DAC is simply the number of bit inputs that a DAC possesses, which indicates the smallest analogue increment that the converter can produce as a fraction of V_{FS}, e.g. 8 bits = 1 part in 2^8 (256). Resolution implies nothing about the accuracy of a DAC, which is defined by linearity and other errors.

1.3.9 Useful Resolution

If an n bit DAC has a differential non-linearity of say −1.5 LSB then it is non-monotonic. However, if the LSB input is made permanently '0' then the DAC becomes an n − 1 bit device with an LSB equal to twice the original LSB. The differential non-linearity error thus becomes −0.75 (new) LSB and the device is monotonic at a resolution of n − 1 bits. This is illustrated in figure 6, which shows the transfer characteristic of a 3-bit DAC that has a useful resolution of 2 bits.

Due to manufacturing tolerances a proportion of n-bit converters will have only n − 1 or n − 2 bit useful resolution. In applications not requiring n −bit useful resolution these reduced resolution versions offer a significant price advantage. The useful resolution of Ferranti DACs is guaranteed over their full operating temperature range.
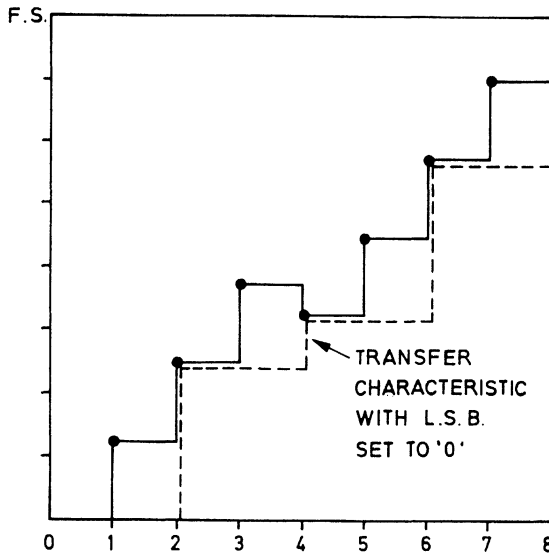
6053

Fig. 6.   Non-monotonic 3-bit DAC With a Useful Resolution of 2 bits

6

1.3.10 Settling Time is the time taken after a transition of the input code for the output of a DAC to settle to within $\pm\frac{1}{2}$ LSB of its final value. This varies depending on which bits are being changed. It may be specified for a change of 1 LSB which generally gives the most optimistic (fastest) figure. More conservative figures are given by the most major transition (where the MSB changes in one direction and all other bits change in the opposite direction, e.g. 01111111 to 10000000 or vice versa) or by a change from all bits off to all bits on (00000000 to 11111111) or vice versa.

1.4   Bipolar Operation

The discussion so far has been concerned only with DACs producing a single polarity (usually positive) output voltage. In some applications a bipolar (both positive and negative) output range may be required.

This can be achieved by adding a negative offset of $\frac{V_{REF}}{2}$ to the analogue output, as shown in figure 7. For all input codes where the MSB is '0' the output voltage is then negative, and for output codes where the MSB is '1' the output voltage is positive. Where the input coding is normally binary but the output voltage is offset by $\frac{-V_{REF}}{2}$ then the input code is referred to as offset binary.

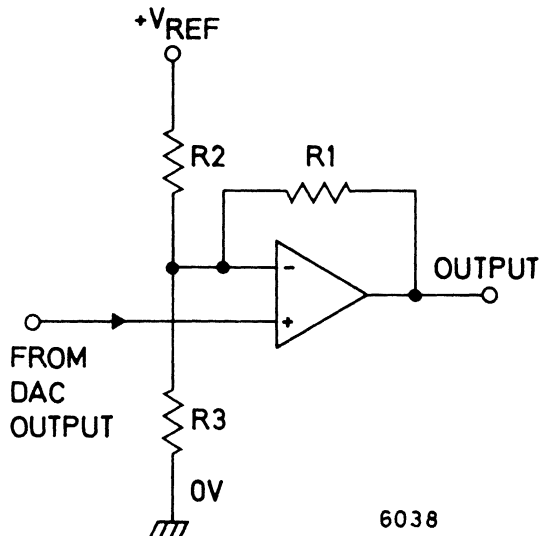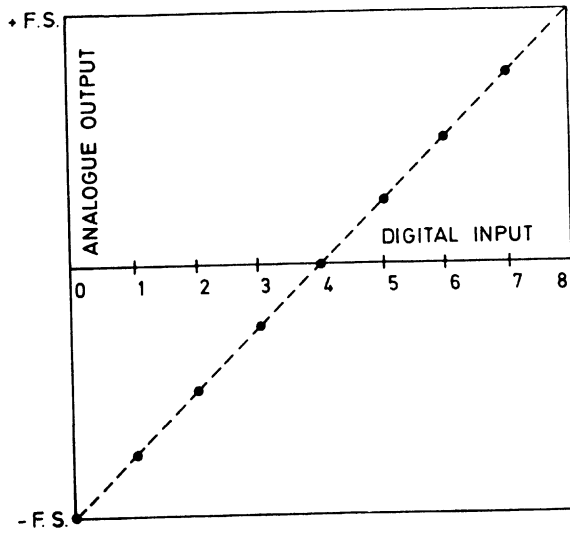The transfer function of a 3-bit DAC with offset binary coding is shown in figure 8.

Fig. 7.   Bipolar Operation of a DAC

D to A Converters

6039

Fig. 8. Bipolar Operation of a 3-bit DAC

2. ANALOGUE TO DIGITAL CONVERTERS

An analogue to digital Converter (ADC) is a device which converts an analogue input into a corresponding digital output code.

2.1 Ideal Output Characteristics

Assuming a unipolar input voltage and binary coded output, the transfer function of an ideal n-bit ADC is given by:

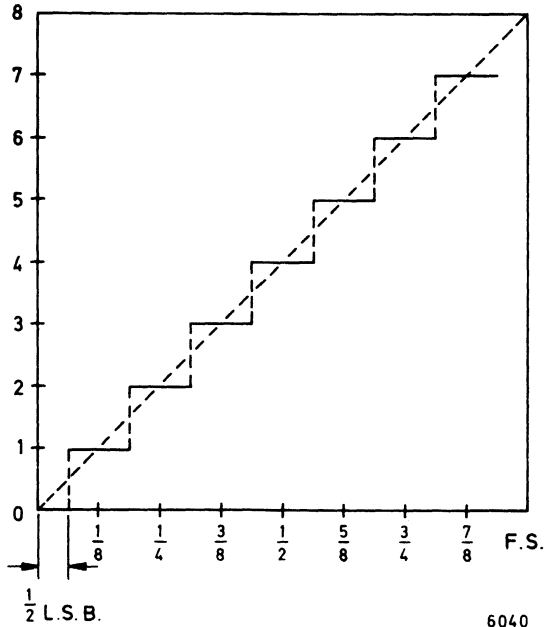$$V_{FS} (B_1.2^{-1} + B_2.2^{-2} + ... + B_n.2^{-n}) = V_{in} \pm \tfrac{1}{2}LSB$$

Fig. 9. Ideal 3-bit ADC Transfer Characteristic

The transfer function of an ideal 3-bit ADC is shown in figure 9. In this case there are 8 digital output codes corresponding to the 8 input codes of a DAC. However, unlike the analogue output of a DAC, the analogue input of an ADC can vary continuously, which means that each digital output code, with the exception of 0 and 7, exists over an analogue increment of 1 LSB. The zero of an ADC is usually trimmed so that the transitions between codes occur $\tfrac{1}{2}$ LSB on either side of the nominal analogue input for a particular code. For example, the nominal input for output code 2 is $\tfrac{1}{4} V_{FS}$. The transition from 1 to 2 occurs at $\tfrac{3}{16} V_{FS}$ and the transition from 2 to 3 occurs at $\tfrac{5}{16} V_{FS}$.

As with a DAC, an 'ideal' straight line may be drawn through the transfer characteristic of an ADC.

9

A to D Converters

2.2 Practical A to D Conversion Methods

There are many methods of performing an analogue to digital conversion. Although not all of these methods are used in the current range of Ferranti A-D converters, they are all, nonetheless, mentioned for the sake of completeness.

2.2.1 Parallel (Flash) Conversion

In an n-bit parallel converter (Fig. 10) a resistor ladder is used to generate $2^n - 1$ voltage levels from 1 LSB to $(2^n - 1) \times$ LSB which are fed to the reference inputs of $2^n - 1$ voltage comparators. The analogue input signal is fed to the second input of each comparator, and is thus compared simultaneously with each of the $2^n - 1$ voltage levels. At the point in the comparator chain where the reference voltage exceeds the input voltage the comparator outputs will change over from low to high. The comparator outputs are encoded into whatever digital output coding is required.
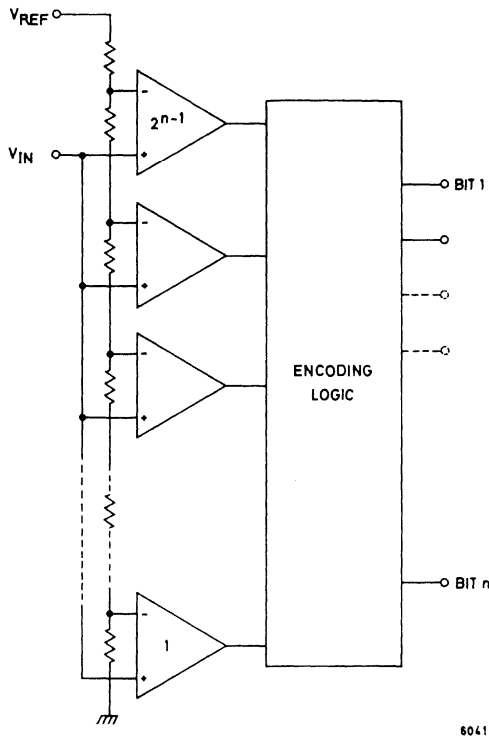

Fig. 10. Parallel A-D Converter

A to D Converters

Since the only delays involved in the conversion are the propagation delay of one comparator plus the logic propagation delays, parallel converters are very fast and may perform in excess of 10 million conversions per second. However, due to the large number of comparators required (63 for a 6-bit converter, 255 for an 8-bit converter) they are expensive to produce. Applications include digital video systems, digital storage oscilloscopes and radar data processing.

2.2.2 Staircase and Comparator

In this type of ADC the input code of a DAC is incremented by a binary counter to give a staircase waveform, as shown in figure 11. This is compared with the analogue input and when the staircase exceeds the analogue voltage the comparator output changes state and stops the clock. The count reached by the binary counter is thus the ADC output code. This method of A to D conversion is relatively simple and cheap, but is also relatively slow, requiring $2^n - 1$ clock pulses for a full scale conversion, where n is the number of bits. This conversion method is used in the ZN425 series of dual-purpose D-A/A-D converters.
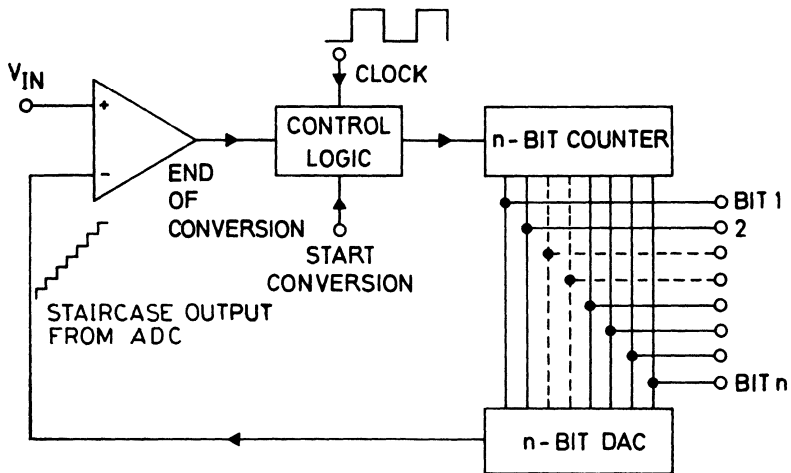

6042

Fig. 11.   Staircase (Ramp) and Compare ADC

A to D Converters

2.2.3 Tracking Converters

As its name implies, a tracking converter can follow changing analogue inputs. The principle operation is similar to that of the staircase and compare type of converter, but it uses an up/down counter and a window comparator, as shown in figure 12. When the DAC output is less than the analogue input the comparator instructs the counter to count up and the DAC output thus increases. If the DAC output is greater than the analogue input the comparator causes the counter to count down, thus decreasing the DAC output. When the DAC output is equal to the analogue input $\pm \frac{1}{2}$ LSB, the input is within the 'window' of the comparator and the counter is stopped. This is illustrated in figure 13. A tracking converter has speed advantages over a staircase and compare type, since the counter of the latter type can only count up, and must therefore be reset between conversions. In the case of a tracking converter, once it has performed an initial conversion starting from zero, any subsequent conversions require only that number of clock pulses necessary to track any increase or decrease in input voltage.
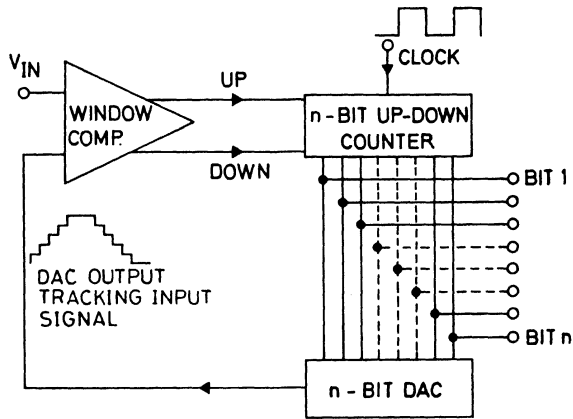
6043

Fig. 12.   Tracking ADC

As an extreme example consider an analogue input that changes from V_{FSO} to (V_{FSO} −1 LSB). The staircase and compare converter will require 2^n −1 clock pulses for the first conversion and 2^n −2 clock pulses for the second conversion. The tracking converter on the other hand, will require 2^n −1 clock pulses for the first conversion but only one clock pulse for the second conversion. This is illustrated in figure 14.
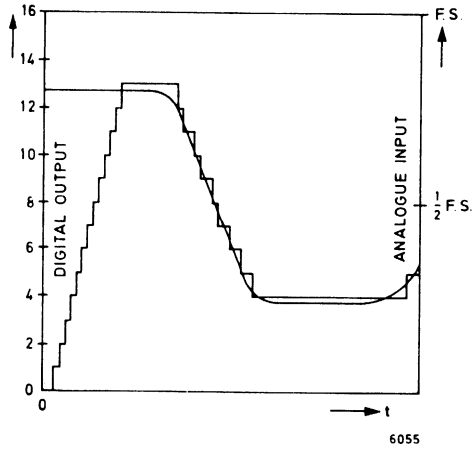
12
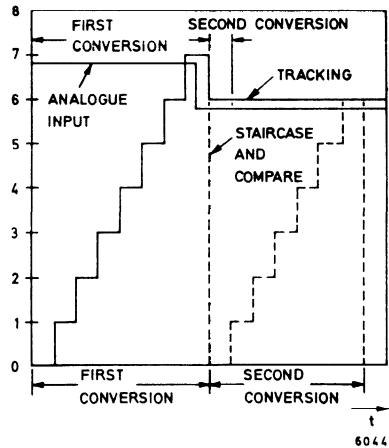
Fig. 13. Operation of Tracking ADC

Fig. 14. Comparison of ramp and compare and tracking ADCs

A to D Converters

In general it can be said that a tracking converter will follow signals whose rate of change is less than ± 1 LSB $\times$ clock frequency. If this condition is met there is no need to use a sample-and-hold circuit on the analogue input.

A tracking technique is used in the ZN433 series of converters.

2.2.4 Successive Approximation Converters

The operation of a staircase and compare ADC is analogous to weighing, say an 11 gramme weight, on a balance by adding one gramme weights until the scale tips, which is clearly a very slow method. A faster procedure, known as successive approximation, uses weights of 16, 8, 4, 2 and 1 grammes. The 16 gramme weight is tried first and is discarded because it tips the scale. The 8 gramme weight is tried next, and is left on the pan. Next the 4 gramme weight is tried and discarded, and the 2 and 1 gramme weights are tried and retained. The final result is the sum of the weights remaining on the scale pan, and the operation has taken 5 'cycles' as opposed to 11 'cycles' for the staircase and compare method.

The principle of a successive approximation ADC is identical. The MSB of a DAC is first set to '1' and the output is compared to the analogue input. If it is greater than the input the MSB is reset to '0', otherwise it is left at '1'. The next bit is then set to '1' and the DAC output is again compared to the analogue input. Again it is either reset or left at '1' depending on the result of the comparison. This procedure is repeated for every bit down to the LSB, and the final input code to the DAC is the output code of the ADC. A successive approximation cycle is illustrated in figure 15.
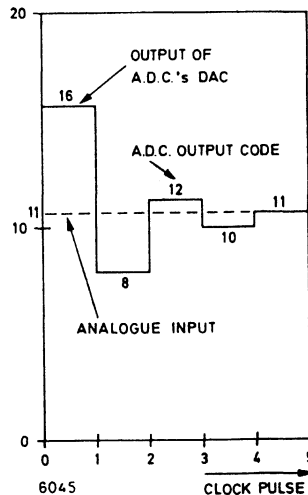
Fig. 15.   Operation of a Successive Approximation ADC

14

Successive approximation is used in the ZN427 and ZN432 series of converters.

2.2.5 Dual Slope Converters

Dual slope integration is one of the slowest methods of A to D conversion, but it offers high resolution at a modest cost.

A block diagram of a dual-slope converter is shown in figure 16. It operates in the following manner: Switch S1 is closed by the control logic, S4 is opened and the input voltage is integrated for n clock periods, where n is usually the maximum count of the counter. At the end of this time the integrator output voltage, V_o, is $\dfrac{-V_{in}\, n\, T_c}{RC}$ where T_c is the clock period. This is shown in figure 17.
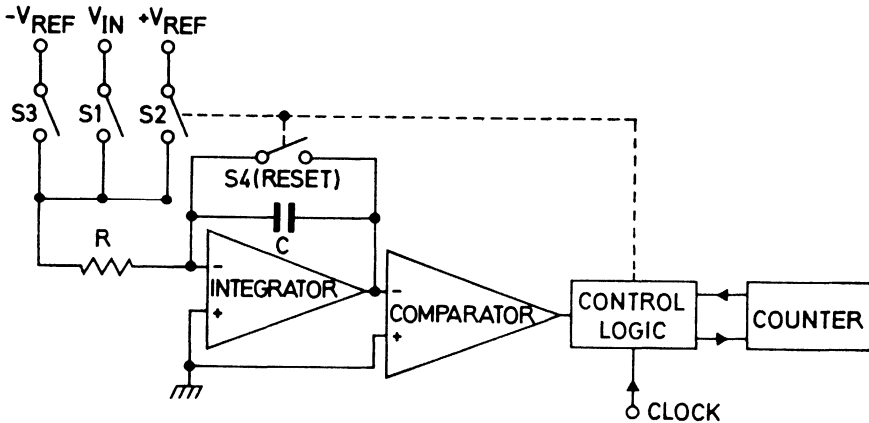
6046

Fig. 16.   Dual-Slope ADC

During this period the polarity of the input signal is detected by the comparator. At the end of the integration period S1 is opened and, depending on the polarity of V_{in}, either S2 or S3 is closed to connect the integrator to a reference voltage of opposite polarity to V_{in}. The counter is now allowed to count from zero until the integrator output reaches 0 volts, when the comparator output changes state and the counter is stopped. Since the integration is over the same voltage range (V_o), $V_o = \dfrac{-V_{REF} \times T_c}{RC}$, where x is the count

15

A to D Converters
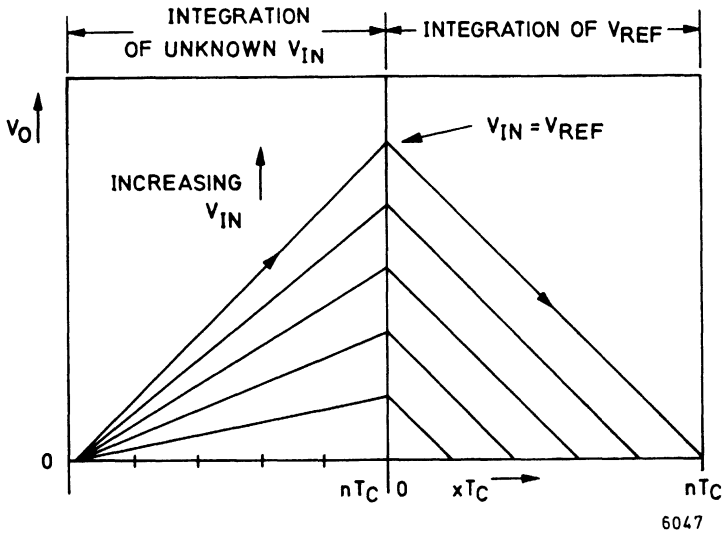
Fig. 17. Operation of Dual-Slope ADC

reached by the time the integrator output crosses zero. Thus

$$\frac{V_{in}.n\,T_c}{RC} = \frac{V_{REF} \times T_c}{RC}$$

$$\text{or } x = \frac{V_{in}.n}{V_{REF}}$$

Since n and V_{REF} are both fixed the output count is proportional to the input voltage. Since both the first and second integrations occur under identical conditions the converter is unaffected by any long-term variations in T_c, R or C, as demonstrated by the disappearance of these terms from the final equation. The only factors affecting the accuracy of the converter are (1) the stability of V_{REF} (2) the stability of the 'on' resistance of S1 to S3 and (3) drift in the integrator and comparator op-amps. These effects can be minimised by careful design.

Dual slope converters are generally used where high resolution and low cost are more important than speed, for example in digital voltmeters.

The ZNA116 and ZNA216 are DVM logic subsystems containing the clock, counter and all control logic necessary for dual slope converter or DVM.

16

2.3 A to D Parameters and Definitions

2.3.1 A to D Converter Errors

Like DACs, practical ADCs are subject to a number of error sources, and since most ADCs contain a reference DAC, many of these error sources are the same for both types of converter.

2.3.2 Quantising Error (Uncertainty)

Quantising error is an ADC specification that has no counterpart in DAC specifications. For each input code of a DAC there is a unique analogue output level, but for any ADC output code there is a 1 LSB range of analogue input levels. It is thus not possible to tell from the output code the precise value of the analogue input level, there being a quantising error or uncertainty of $\pm\frac{1}{2}$ LSB. Since all ADCs have this inherent quantising error the parameter is frequently not quoted in specifications.

2.3.3 Missing Codes

Missing codes are perhaps best explained by considering the operation of a staircase and compare type 3-bit ADC which has a non-monotonic DAC, as shown in figure 18. The reference DAC exhibits non-monotonicity at input code 4, i.e. step 4 of the staircase decreases. There is thus no way in which the counter can be stopped at this code. If the analogue input is less than the DAC output for code 3 then the comparator will stop the counter before 4 is reached. If the analogue input is greater than output 3 it must also be greater than output 4, so the comparator will not change state at code 4.
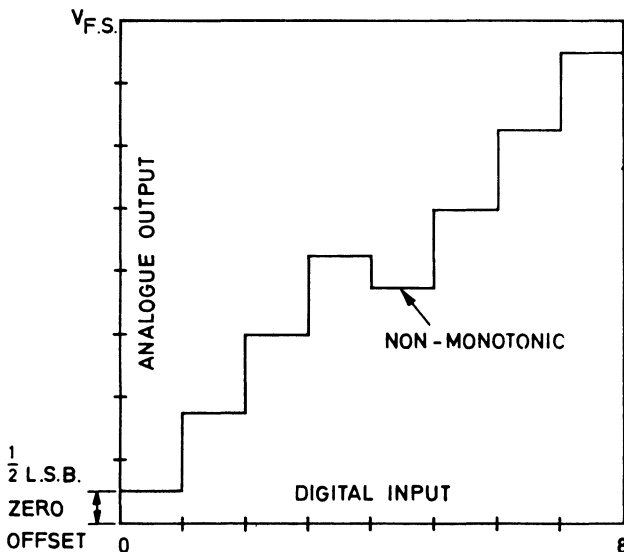
Fig. 18. Non-monotonic DAC used in an ADC

17

A to D Converters

Output code 4 will thus never appear and is known as a 'missing' code. The transfer function of an ADC with a missing code is shown in figure 19.
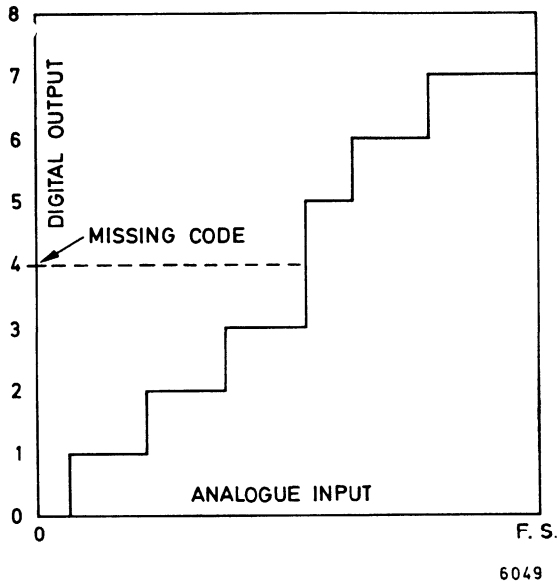
Fig. 19. ADC With Missing Code

2.3.4 Zero Transition

As explained earlier, the zero of an ADC is usually trimmed so that the output transition from 0 to 1 occurs at an input level corresponding to $\frac{1}{2}$ LSB, i.e. $\frac{1}{2}\frac{V_{FS}}{2^n}$. However, as supplied the reference DAC of an ADC I.C. will not have the $\frac{1}{2}$ LSB offset necessary to achieve this. The zero transition will thus occur at 1 LSB plus the DAC zero error, plus the comparator offset voltage. These three parameters are frequently lumped together as the (untrimmed) zero transition of the ADC.

2.3.5 Gain Error

This is the difference between the slope of a line drawn between the actual zero and full scale transition points and that of a line drawn through the ideal transition points.

2.3.6 Non-linearity (Linearity Error)

Non-linearity is the maximum amount by which any actual transition points deviates from the corresponding ideal transition point. It is specified as a percentage of full-scale or a fraction of an LSB. A linearity error of less than $\pm\frac{1}{2}$ LSB assures no missing codes.

18

2.3.7 Differential Non-linearity

This is the maximum difference between any 1 LSB increment of the analogue input and the ideal size of an LSB increment $\frac{V_{FS}}{2^n}$. Differential non-linearity of less than 1 LSB guarantees no missing codes.

2.3.8 Resolution

The resolution of an ADC is simply the number of bit outputs that the converter possesses. As with a DAC, resolution implies nothing about the accuracy of a device.

2.3.9 Useful Resolution

Useful resolution is the resolution (number of bits) at which an ADC has no missing codes, which for Ferranti ADCs is guaranteed over the operating temperature range. As with DACs, an n-bit ADC may have a useful resolution less than n bits, for reasons previously explained.

2.3.10 Conversion Time

The time taken for an ADC to perform a complete conversion is known as the conversion time. For successive approximation converters conversion time is fixed by the number of bits and the clock frequency. However, for other types, conversion time may vary with input voltage. For example, a ramp and compare ADC requires $2^n -1$ clock pulses for a full scale conversion but only one clock pulse for a one bit conversion. It is thus important to check exactly what is being specified.

2.4 Bipolar Operation

As with a DAC, an ADC may be used for bipolar operation. Taking the ZN427 as an example the input is offset by $\frac{+V_{REF}}{2}$ so that the input voltage presented to the ADC is always positive, even with negative input voltages down to $\frac{-V_{REF}}{2}$. The principle of offsetting an ADC input is illustrated in figure 20, whilst the transfer function of a 3 bit bipolar ADC is shown in figure 21. In this case the **output** coding is known as offset binary.

A to D Converters
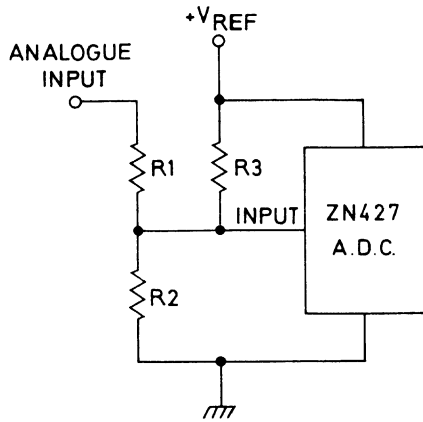
6050

Fig. 20.   Bipolar Operation of an ADC
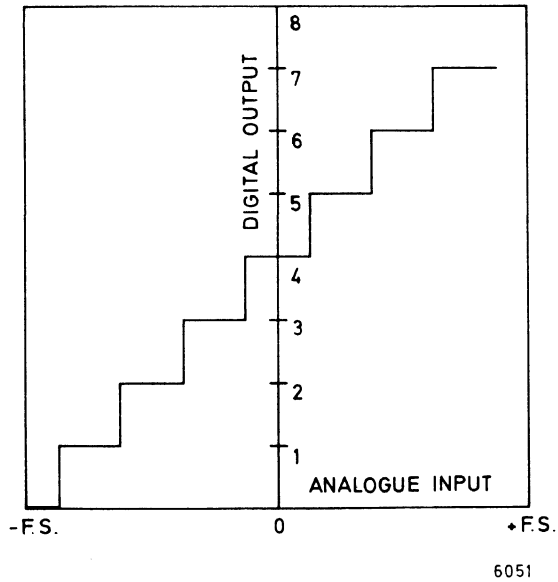
6051

Fig. 21.   Bipolar Transfer Characteristic of an ADC

3. COMPANDING CONVERTERS

Unlike conventional DACs whose outputs are invariably linearly proportional to the digital number at the inputs, a companding DAC has an output that is intentionally non-linear with respect to its digital input.

In general, assuming a constant reference, a companding DAC's output is an exponential function of the digital input. A small change in the digital input, when it is near zero, produces a very small change in the analogue output. As the digital input goes towards full scale, the same digital change produces a progressively larger change in the analogue output.

A companding DAC's transfer function is an eight segment piecewise linear approximation to the ideal exponential characteristic. Within each segment – also called a 'chord' – the transfer function is linear. However, with the sizes of the analogue-output steps differing by a factor of two in adjacent chords, the chords have slopes that approximate the non-linear function. Each chord contains 16 steps making a total of 128 steps in all from zero to full scale.

Companding DACs usually relate to 7-bit resolution with an additional sign bit making it an 8-bit input device. The sign bit is the MSB, the next three most significant bits selecting the chord and the final four bits the steps within the chord. The final transfer characteristic is shown in figure 22. The ADC companding function is similar in nature, with the transfer characteristic being the inverse of that shown for the DAC.

Fig. 22. Transfer Function of a Companding DAC

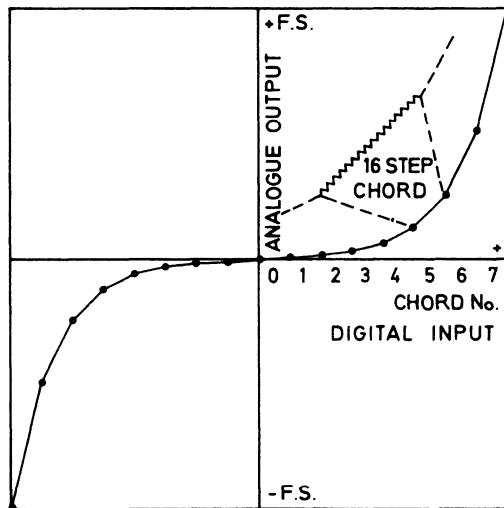The most popular application areas for this type of converter are single channel code conversion of voice signals in telephone exchange networks. The Ferranti ZNPCM1 Codec performs such a function using some innovative circuit techniques. The companding is performed in all digital circuitry using an intermediate delta-sigma modulation function.

4. QUALITY ASSURANCE PROGRAMME

The quality control procedures at Ferranti Electronics Limited are based on British Standard 9000, the relevant documents being:

BS 9002: Qualified products list for electronic components of assessed quality (including list of approved firms).

BS 9400: Integrated electronic circuits and micro-assemblies of assessed quality.

BS 9450: Custom-built integrated circuits of assessed quality.

BS 6001: Sampling procedures and tables for inspection by attributes.

The quality emphasis at Ferranti is on process control (as indicated by the use of many monitors and audits) in addition to gate inspections. This philosophy is consistent with building in quality and reliability rather than attempting solely to screen for it.

There are five basic stages in the manufacture of Ferranti data converters, as shown below:

1 Material Processing	→	2 Assembly	→	3 Screening	→	4 Testing	→	5 Quality Assurance
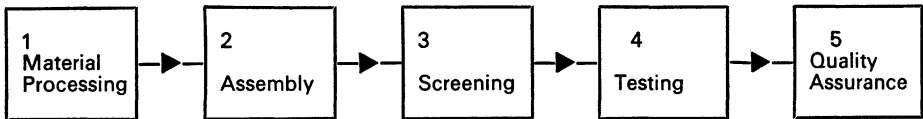
Each of these stages has associated with it a number of quality control checks to ensure that components will meet the standards required by the most stringent environments encountered in the field of electronics.

4.1 Processing

The technology used to fabricate the Ferranti range of data converters is a five mask bipolar process (see publication ref. ESA 480673). This process is used to manufacture the whole range of Ferranti LSI products, but is especially suited to converter products since it allows analogue and digital circuits to be fabricated on the same chip, with good yields and high packing densities. The process has full BS 9450 capability approval and is the first bipolar process in the U.K. to receive such approval.

4.2 Assembly

Ferranti data converters are available in either moulded or hermetically sealed ceramic dual in-line (DIL) packages (though certain types are available only in ceramic package). The assembly flow-charts for both types of package are shown in Table 1. All products are manufactured by the same routes and using the same techniques as BS 9000 approved products.

22

Q A Programme

TABLE 1

PLASTIC	CERAMIC
Wafer ▽	Wafer ▽
◯ Dice Preparation	◯ Dice Preparation
◇ Dice Inspection	◇ Dice Inspection
◯ Alloy	☐ QC Lot Acceptance
◯ Bond	◯ Alloy
◇ Pre-cap Inspection	◯ Bond
☐ QC Lot Acceptance	◇ Pre-cap Inspection
◯ Mould	☐ QC Lot Acceptance
◯ Post Mould Cure(5 Hrs. at 185°C)	◯ Bake 1 hour at 200°C
◯ Tin plate	◯ Encapsulate
☐ Visual Quality & Solderability	☐ Fine Leak Test
◯ Part Mark	☐ Gross Leak Test
☐ Part Mark Quality & Durability	◯ Part Mark
◇ Physical Inspection	☐ Part Mark Quality & Durability
☐ QC Lot Acceptance	◇ Physical Inspection
◯ Electrical Test	☐ QC Lot Acceptance
▽ Warehouse	◯ Electrical Test
	▽ Warehouse

Key: ◯ Product Process   ◇ 100% Inspection   ☐ Sampling

6083

23

Q A Programme

TABLE 2

```
                    ┌─────────────────────────────────┐
                    │   PRODUCTION BATCH FORMED        │
                    └─────────────────────────────────┘
```

CATEGORY S2 Screening Level B	CATEGORY S3 Screening Level C
Pre-cap inspection BS 9400 1.2.10 level B	Pre-cap inspection BS 9400 1.2.10 level B
High Temperature Storage BS 9400 1.2.6.3 150°C for 24 hours	High Temperature Storage BS 9400 1.2.6.3 150°C for 24 hours
Rapid Change of Temperature BS 9400 1.2.6.13 10 cycles −65°C to +150°C	Rapid Change of Temperature BS 9400 1.2.6.13 10 cycles −65°C to +150°C
Acceleration Steady State BS 9400 1.2.6.9 294000 m/s². Direction Y1	Acceleration Steady State BS 9400 1.2.6.9 294000 m/s². Direction Y1
Fine and Gross Leak Tests BS 9400 1.2.6.14	Fine and Gross Leak Tests BS 9400 1.2.6.14
Electrical Tests at 25°C as per subgroups A2, A3(a)	
Burn-in Screen BS 9400 1.2.9.2 160 hours minimum at 125°C	
Final Electrical Tests at 25°C as per subgroups A2, A3(a)	Final Electrical Tests at 25°C as per subgroups A2, A3(a)

4.3 Screening

In addition to the standard manufacturing cycle, optional screening procedures are available to produce high-reliability products. A full breakdown of the options available, related to their BS 9400 procedures, is shown in Table 2.

4.4 Testing

On completion of assembly all devices are subjected to 100% functional and d.c. testing in addition to either an S4, 2.5% sample or 100% check on a.c. characteristics depending on device type. The d.c. tests are inset to tighter limits than those shown on the data sheet in order to ensure that the device will function within the specified conditions over its full operating temperature range.

In addition to the 100% test already described, devices manufactured to commercial specifications also undergo sample tests to the AQLs in Table 3, including the temperature extreme tests mentioned above.

TABLE 3

Inspected Parameter	Inspection Level	AQL
Visual & Mechanical including major external workmanship and marking permanency	I	1%
Function	II	0.15%
Major Electrical Parameters at $T_{amb} = 25°C$	II	0.65%
Major Electrical Parameters over operating temperature range	II	2.5%

4.5 Quality Assurance

Despite all the measures taken to ensure that commercial product is of a high standard it is inevitable that certain market sectors will require a higher level of quality assurance. These market sectors are predominantly military and telecommunications orientated.

Wherever devices are supplied to these more stringent QA requirements they are re-routed at the end of the assembly cycle through our QA Bond Department. They are subjected, on a lot-by-lot basis, to a more rigorous examination of ther quality using methods laid down in BS 9000 or its equivalent for the specification concerned.

In addition to lot-by-lot testing, long term life testing of product is performed continually. This enables constant monitoring of process stability and any undesirable deviations from the norm are quickly brought to light so that corrective measures may be implemented.

Q A Programme

4.6 Acceptable Quality Levels

As explained earlier the procedures and manufacturing techniques used by Ferranti are consistent with producing an inherently reliable product rather than screening out unreliable product. This is achieved by careful process control combined with numerous gate inspections.

In order for such a system to be effective it is necessary to implement a sampling procedure where the sample size and inspection levels of the various stages are adequate to assure satisfactory quality of the end product whilst remaining cost effective. This can be achieved only after a long history of semiconductor manufacture, which gives an intimate knowledge of the problems likely to arise at each stage of manufacture, and the best methods of inspecting for them.

The sampling procedures used by Ferranti are those outlined in BS 6001. The Acceptable Quality Level (AQL) is the maximum percentage of defective devices that can, for the purposes of inspection, be considered satisfactory as a process average.

The AQL sample size codes and sampling plan used by Ferranti are reproduced in tables 4 and 5.

TABLE 4
SAMPLE SIZE CODE LETTERS

Lot or batch size			Special inspection levels				General inspection levels		
			S-1	S-2	S-3	S-4	I	II	III
2	to	8	A	A	A	A	A	A	B
9	to	15	A	A	A	A	A	B	C
16	to	25	A	A	B	B	B	C	D
26	to	50	A	B	B	C	C	D	E
51	to	90	B	B	C	C	C	E	F
91	to	150	B	B	C	D	D	F	G
151	to	280	B	C	D	E	E	G	H
281	to	500	B	C	D	E	F	H	J
501	to	1200	C	C	E	F	G	J	K
1201	to	3200	C	D	E	G	H	K	L
3201	to	10000	C	D	F	G	J	L	M
10001	to	35000	C	D	F	H	K	M	N
35001	to	150000	D	E	G	J	L	N	P
150001	to	500000	D	E	G	J	M	P	Q
500001	and	over	D	E	H	K	N	Q	R

Q. A Programme – TABLE 5

Acceptable Quality Levels (normal inspection)

Sample size code letter	Sample size	0.010	0.015	0.025	0.040	0.065	0.10	0.15	0.25	0.40	0.65	1.0	1.5	2.5	4.0	6.5	10	15	25	40	65	100	150	250	400	650	1000
		Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re
A	2	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	0 1	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31
B	3	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	0 1	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31	44 45
C	5	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	0 1	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31	44 45	⇧
D	8	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	0 1	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31	44 45	⇧	⇧
E	13	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	0 1	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31	44 45	⇧	⇧	⇧
F	20	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	0 1	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31	44 45	⇧	⇧	⇧	⇧
G	32	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	0 1	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31	44 45	⇧	⇧	⇧	⇧	⇧
H	50	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	0 1	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31	44 45	⇧	⇧	⇧	⇧	⇧	⇧
J	80	⇩	⇩	⇩	⇩	⇩	⇩	⇩	⇩	0 1	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31	44 45	⇧	⇧	⇧	⇧	⇧	⇧	⇧
K	125	⇩	⇩	⇩	⇩	⇩	⇩	⇩	0 1	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31	44 45	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧
L	200	⇩	⇩	⇩	⇩	⇩	⇩	0 1	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31	44 45	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧
M	315	⇩	⇩	⇩	⇩	⇩	0 1	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31	44 45	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧
N	500	⇩	⇩	⇩	⇩	0 1	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31	44 45	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧
P	800	⇩	⇩	⇩	0 1	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31	44 45	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧
Q	1250	⇩	⇩	0 1	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31	44 45	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧
R	2000	⇩	0 1	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31	44 45	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧	⇧

⇩ = Use first sampling plan below arrow. If sample size equals, or exceeds, lot or batch size, do 100 percent inspection.
⇧ = Use first sampling plan above arrow.
Ac = Acceptance number.
Re = Rejection number.

28

5. PRODUCT SELECTION GUIDE — D TO A CONVERTERS

Type	Useful Resolution (bits)	Setting Time (μs)	On-Chip Ref	Input Latch	Temperature Range (°C)	Features	Page
ZN425E-6	6	1	Yes	—	0 to +70	D to A with on-chip counter	31
ZN426E-6	6	1	Yes	—	0 to +70	TTL and CMOS compatible	39
ZN429E-6	6	1	—	—	0 to +70	Low cost, TTL and CMOS compatible	71
ZN425E-7	7	1	Yes	—	0 to +70	D to A with on-chip counter	31
ZN426E-7	7	1	Yes	—	0 to +70	TTL and CMOS compatible	39
ZN429E-7	7	1	—	—	0 to +70	Low cost, TTL and CMOS compatible	71
ZN425E-8 ZN425J-8	8 8	1 1	Yes Yes	— —	0 to +70 −55 to +125	D to A with on-chip counter	31
ZN426E-8 ZN426J-8	8 8	1 1	Yes Yes	— —	0 to +70 −55 to +125	TTL and CMOS compatible	39
ZN428E-8 ZN428J-8	8 8	0.8 0.8	Yes Yes	Yes Yes	0 to +70 −55 to +125	Microprocessor, TTL and CMOS compatible	61
ZN429E-8 ZN429J-8	8 8	1 1	— —	— —	0 to +70 −55 to +125	Low cost, TTL and CMOS compatible	71
ZNPCM1E ZNPCM1J	— —	— —	— —	— —	0 to +70	Single Channel Codec	127

Product Selection Guide - A to D Converters

Type	Useful Resolution (bits)	Conversion Time (µs)	Conversion Method	On-Chip Ref	Temperature Range (°C)	Features	Page
ZN425E-6	6	1000	Ramp and Compare	Yes	0 to +70	Low Cost Dual Purpose A-D/D-A Converter	31
ZN425E-7	7	1000	"	Yes	0 to +70		
ZN425E-8	8	1000	"	Yes	0 to +70		
ZN425J-8	8	1000	"	Yes	−65 to +125		
ZN427E-8	8	10	Successive Approx.	Yes	0 to +70	Microprocessor, TTL and CMOS compatible	47
ZN427J-8	8	10	"	Yes	−55 to +125		
ZN432CJ-8	8	15	Successive Approx.	Yes	0 to +70	TTL and CMOS compatible Serial Output	77
ZN432BJ-8	8	15	"	Yes	−45 to +85		
ZN432J-8	8	15	"	Yes	−55 to +125		
ZN433CJ-8	8	1	Tracking	Yes	0 to +70	TTL and CMOS compatible Serial Output	87
ZN433BJ-8	8	1		Yes	−45 to +85		
ZN433J-8	8	1		Yes	−55 to +125		
ZN432CJ-9	9	15	Successive Approx.	Yes	0 to +70	TTL and CMOS compatible Serial Output	77
ZN432BJ-9	9	15		Yes	−45 to +85		
ZN432J-9	9	15		Yes	−55 to +125		
ZN433CJ-9	9	1	Tracking	Yes	0 to +70	TTL and CMOS compatible Serial Output	87
ZN433BJ-9	9	1		Yes	−45 to +85		
ZN433J-9	9	1		Yes	−55 to +125		
ZN432CJ-10	10	15	Successive Approx.	Yes	0 to +70	TTL and CMOS compatible Serial Output	77
ZN432BJ-10	10	15		Yes	−45 to +85		
ZN432J-10	10	15		Yes	−55 to +125		
ZN433CJ-10	10	1	Tracking	Yes	0 to +70	TTL and CMOS compatible Serial Output	87
ZN433BJ-10	10	1		Yes	−45 to +85		
ZN433J-10	10	1		Yes	−55 to +125		
ZNA116E	3½ Digit BCD	160 ms	Dual Slope	—	0 to +70	DVM Logic Subsystem	97
ZNA216E	3¾ Digit BCD	160 ms	Dual Slope	—	0 to +70	DVM Logic Subsystem	111
ZNA216J	3¾ Digit BCD	160 ms		—	0 to +70		
ZNPCM1E	—	—	—	—	—	Single Channel Codec	127
ZNPCM1J	—	—		—	—		

7. **FERRANTI semiconductors**

ZN425 Series

8 Bit Monolithic D to A/A to D Converter

FEATURES

- **8, 7 and 6 bit Accuracy**
- **0°C to +70°C (ZN425E Series)**
- **–55°C to +125°C (ZN425J-8)**
- **TTL and 5V CMOS Compatible**
- **Single +5V Supply**
- **Settling Time (D to A) 1 μsec Typical**
- **Conversion Time (A to D) 1 msec typical, using ramp and compare.**

- **Extra Components Required**

    D-A : Reference capacitor (direct   **A-D** : Comparator, gate, clock
    voltage output through   and reference capacitor
    10 kΩ typ.)

DESCRIPTION

The ZN425 is a monolithic 8-bit digital to analogue converter containing an R-2R ladder network of diffused resistors with precision bipolar switches, and in addition a counter and a 2.5V precision voltage reference. The counter is a powerful addition which allows a precision staircase to be generated very simply merely by clocking the counter.

Fig. 1 – System Diagram

31
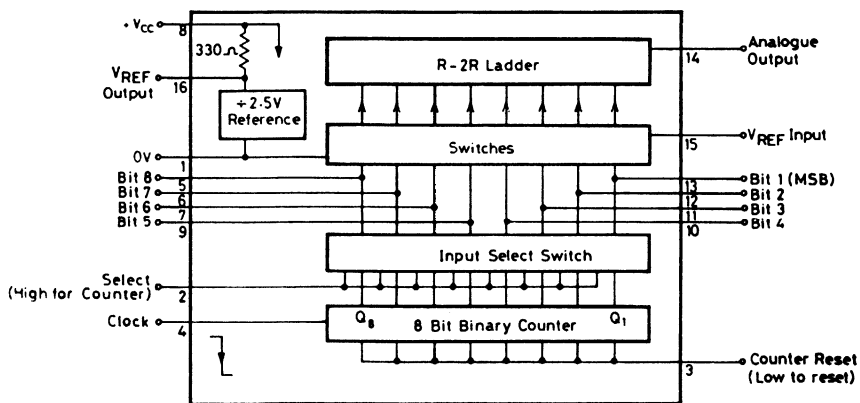
ZN425 Series

INTRODUCTION

The ZN425 is an 8-bit dual mode digital to analogue/analogue to digital converter. It contains an 8-bit D to A converter using an advanced design of R-2R ladder network and an array of precision bipolar switches plus an 8-bit binary counter and a 2.5 volt precision voltage reference all on a single monolithic chip.

The special design of ladder network results in full 8-bit accuracy using normal diffused resistors.

The use of the on-chip reference voltage is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted.

By including on the chip an 8-bit binary counter, analogue to digital conversion can be obtained simply by adding an external comparator (ZN424P) and clock inhibit gating (ZN7400E).

By simply clocking the counter the ZN425 can be used as a self-contained precision ramp generator.

A logic input select switch is incorporated which determines whether the precision switches accept the outputs from the binary counter or external digital inputs depending upon whether the control signal is respectively high or low.

The converter is of the voltage switching type and uses an R-2R resistor ladder network as shown in Fig. 2.

Fig. 2 – The R-2R Ladder Network

Each 2R element is connected either to 0V or V_{REF} by transistor switches specially designed for low offset voltage (typically 1 millivolt).

Binary weighted voltages are produced at the output of the R-2R ladder, the value depending on the digital number applied to the bit inputs.

ORDERING INFORMATION

Operating Temperature	8-bit Accuracy	7-bit Accuracy	6-bit Accuracy	Package
0°C to +70°C	ZN425E-8	ZN425E-7	ZN425E-6	Plastic
–55°C to +125°C	ZN425J-8	—	—	Ceramic

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC} .. .. +7·0 volts

Max. voltage, logic and V_{REF} inputs .. .. +5·5 volts *See note 3*

Operating temperature range .. .. .. 0°C to +70°C (ZN425E Series)
−55°C to +125°C (ZN425J-8)

Storage temperature range .. .. −55°C to +125°C

CHARACTERISTICS (at $T_{amb} = 25\,°C$ and $V_{CC} = +5$ volts unless otherwise specified).

Internal voltage reference

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output voltage	V_{REF}	2·4	2·55	2·7	volts	I = 7·5 mA (internal)
Slope resistance	R_s	—	2	4	ohms	I = 7·5 mA (internal)
V_{REF} Temperature coefficient		—	40	—	ppm/°C	I = 7·5 mA (internal)

Note: The internal reference requires a 0·22 μF stabilising capacitor between pins 1 and 16.

8-Bit D to A Converter and Counter

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Resolution		8	—	—	bits	
Accuracy ZN425J-8 (useful ZN425E-8 resolution) ZN425E-7 ZN425E-6		8 8 7 6	— — — —	— — — —	bits bits bits bits	V_{REF} Input = 2 to 3V
Non-linearity		—	—	±0·5	L.S.B.	*See Note 3*
Differential non-linearity		—	±0·5	—	L.S.B.	*See Note 6*
Settling time		—	1·0	—	μs	1 L.S.B. step
Settling time to 0·5 L.S.B.		—	1·5	2·5	μs	All bits ON to OFF or OFF to ON

Offset voltage   ZN425J-8
             ZN425E-8⎫
             ZN425E-6⎬
             ZN425E-7⎭
	V_{OS}	—
		
		—
			8
			
			3
				12
				
				8
					mV
					
					mV
						All bits OFF
						See Note 3

Full scale output		2·545	2·550	2·555	volts	All bits ON Ext. V_{REF}=2·56V
Full scale temperature coeff.		—	3	—	ppm/°C	Ext. V_{REF}=2·56V
Non-linearity error temp. coeff.		—	7·5	—	ppm/°C	Relative to F.S.R.
Analogue output resistance	R_o	—	10	—	kΩ	
External reference voltage		0	—	3·0	volts	
Supply voltage	V_{CC}	4·5	—	5·5	volts	*See Note 3*
Supply current	I_s	—	25	35	mA	
High level input voltage	V_{IH}	2·0	—	—	volts	*See Notes 1 and 2*
Low level input voltage	V_{IL}	—	—	0·7	volts	

ZN425 Series

CHARACTERISTICS *(continued).*

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
High level input current	I_{IH}	—	—	10	µA	V_{CC} = max. $V_I = 2 \cdot 4V$
		—	—	100	µA	V_{CC} = max. $V_I = 5 \cdot 5V$
Low level input current, bit inputs	I_{IL}	—	—	$-0 \cdot 68$	mA	V_{CC} = max. $V_I = 0 \cdot 3V$
Low level input current, clock reset and input select	I_L	—	—	$-0 \cdot 18$	mA	
High level output current	I_{OH}	—	—	-40	µA	
Low level output current	I_{OL}	—	—	$1 \cdot 6$	mA	
High level output voltage	V_{OH}	$2 \cdot 4$	—	—	volts	V_{CC} = min. Q = 1 $I_{load} = -40$ µA
Low level output voltage	V_{OL}	—	—	$0 \cdot 4$	volts	V_{CC} = min. Q = 0 $I_{load} = 1 \cdot 6$ mA
Maximum counter clock frequency	f_c	3	5	—	MHz	*See Note 5*
Reset pulse width	t_R	200	—	—	ns	*See Note 4*

Notes:

1. The Input Select pin (2) must be held low when the bit pins (5, 6, 7, 9, 10, 11, 12 and 13) are driven externally.

2. To obtain counter outputs on bit pins the Input Select pin (2) should be taken to $+V_{CC}$ via a 1 kΩ resistor.

3. The ZN425J differs from the ZN425E in the following respects:

    (a) For the ZN425J, the maximum linearity error may increase to ±1 LSB over the tempera-ture ranges −55°C to 0°C and +70°C to +125°C.

    (b) Maximum operating voltage. Between 70°C and 125°C the maximum supply voltage is reduced to 5.0V.

    (c) Offset voltage. The difference is due to package lead resistance. This offset will normally be removed by the setting up procedure, and because the offset temperature coefficient is low, the specified accuracy will be maintained.

4. The device may be reset by gating from its own counter.

5. F_{max} in A/D mode is 300 kHz, see page 36.

6. Monotonic over full operating temperature range at resolution appropriate to accuracy.

If Pin 2 is high then the output equals the Q output of the corresponding counter.

If Pin 2 is low then the output transistor, Tr1 is held off.
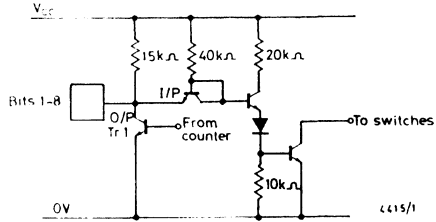
Fig. 3 – Bit Inputs/Outputs

APPLICATIONS

1. 8-bit D to A Converter

The ZN425 gives an analogue voltage output directly from pin 14 therefore the usual current to voltage converting amplifier is not required. The output voltage drift, due to the temperature coefficient of the Analogue Output Resistance R_o, will be less than $0 \cdot 004\%$ per °C (or 1 L.S.B./100°C) if R_L is chosen to be $\geqslant 650$ kΩ.

In order to remove the offset voltage and to calibrate the converter a buffer amplifier is necessary. Fig. 4 shows a typical scheme using the internal reference voltage. To minimise temperature drift in this and similar applications the source resistance to the inverting input of the operational amplifier should be approximately 6 kΩ. The calibration procedure is as follows:

i. Set all bits to OFF (low) and adjust R_2 until $V_{out} = 0 \cdot 000$V.

ii. Set all bits to ON (high) and adjust R_1 until $V_{out} =$ Nominal full scale reading $- 1$ L.S.B.

iii. Repeat *i.* and *ii.*

$$\text{e.g. Set F.S.R. to} +3 \cdot 840 \text{ volts} - 1 \text{ L.S.B.}$$
$$= 3 \cdot 825 \text{ volts}$$
$$\left(1 \text{ L.S.B.} = \frac{3 \cdot 84}{256} = 15 \cdot 0 \text{ millivolts.}\right)$$
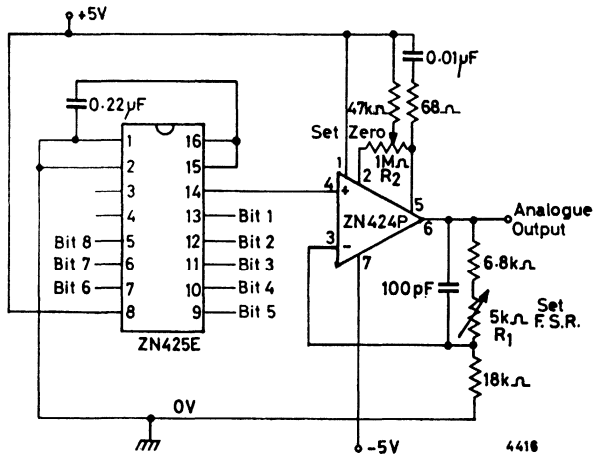
Fig. 4 – 8-bit Digital to Analogue Converter

ZN425 Series

2. 8-bit Analogue to Digital Converter

A counter type ADC can be constructed by adding a voltage comparator and a latch as in Fig. 5. On the negative edge of the CONVERT COMMAND pulse (15 μs minimum) the counter is set to zero and the STATUS latch to logical 1. On the positive edge the gate is opened, enabling clock pulses to be fed to the counter input of the ZN425. The minimum negative clock pulse width to the ZN425 is 100 ns. The analogue output of the ZN425 ramps until it equals the voltage on the other input of the comparator. At this point the comparator output goes low and resets the STATUS latch to inhibit further clock pulses. The logical 0 from the status latch indicates that the 8 bit digital output is a valid representation of the analogue input voltage.

A small capacitor of 47 pF is added to the ZN425 output to stop any positive going glitches prematurely resetting the status latch. This capacitance is in parallel with the ZN425 output capacitance (20–30 pF) and they form a time constant with the ZN425 output resistance (10 kΩ). This time constant is the main limit to the maximum clock frequency. With a fast comparator the clock frequency can be up to 300 kHz. Using the ZN424P as a comparator the clock frequency should be restricted to 100 kHz. The conversion time varies with the input, being a maximum for full scale input.

$$\text{Maximum conversion time} = \frac{256}{\text{clock frequency in Hz}} \text{ seconds}$$
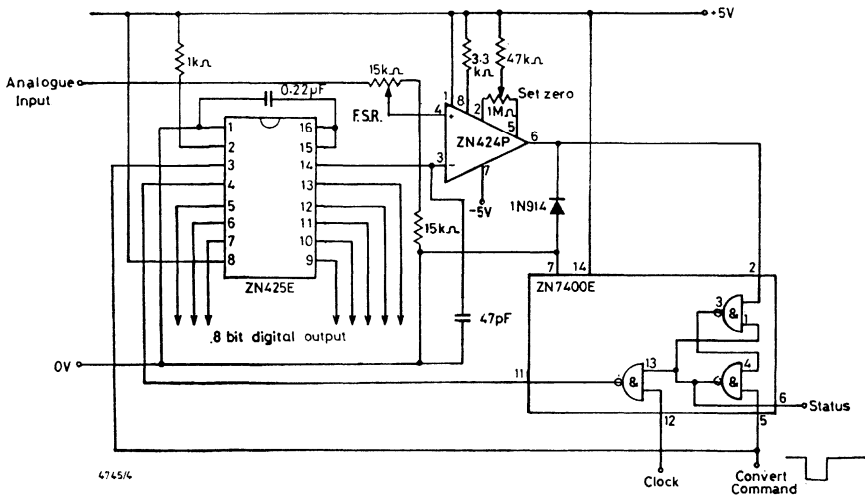
Fig. 5 – 8-bit Analogue to Digital Converter

3. Precision Ramp Generator

The inclusion of an 8-bit binary counter on the chip gives the ZN425 a useful ramp generator function. The circuit, Fig. 6 uses the same buffer stages as the D to A converter. The calibration procedure is also the same. Holding pin 2 low will set all bits to ON and if RESET is taken low with pin 2 high all the bits are turned OFF. If the end voltages of the ramp are not required to be set accurately then the buffer stage could be omitted and the voltage ramp will appear directly at pin 14.
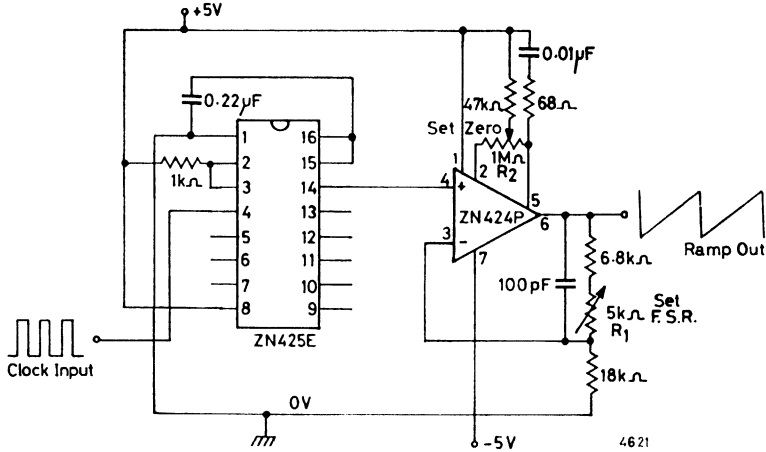
Fig. 6 – Precision Ramp Generator

4. Alternative Output Buffer using the ZLD741

The following circuit, employing the ZLD741 operational amplifier, may be used as the output buffer for both the 8-bit Digital to Analogue Converter (Fig. 4) and the Precision Ramp Generator (Fig. 6).
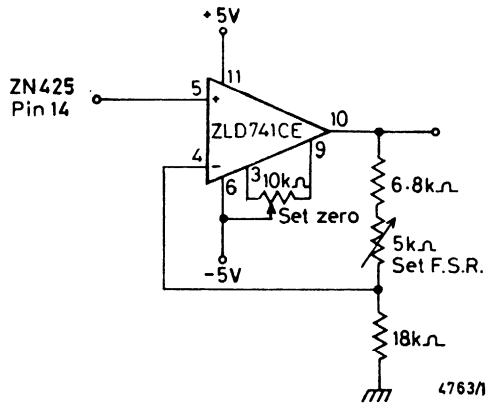
Fig. 7 – The ZLD741 as Output Buffer

5. Further Applications

Details of a wide range of additional applications, described in the Ferranti publication 'Application Report–ZN425 8-bit A-D/D-A Converter', are also available.

37

ZN425 Series

PIN CONNECTIONS
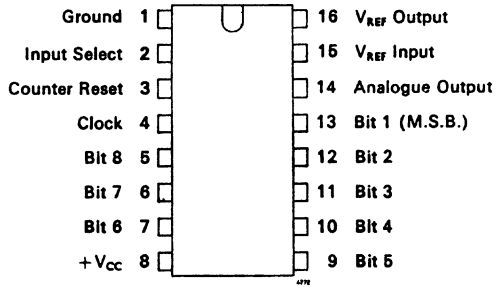
Ground	1	16	V_{REF} Output
Input Select	2	15	V_{REF} Input
Counter Reset	3	14	Analogue Output
Clock	4	13	Bit 1 (M.S.B.)
Bit 8	5	12	Bit 2
Bit 7	6	11	Bit 3
Bit 6	7	10	Bit 4
+V_{CC}	8	9	Bit 5

CHIP DIMENSIONS AND LAYOUT

38

FERRANTI semiconductors
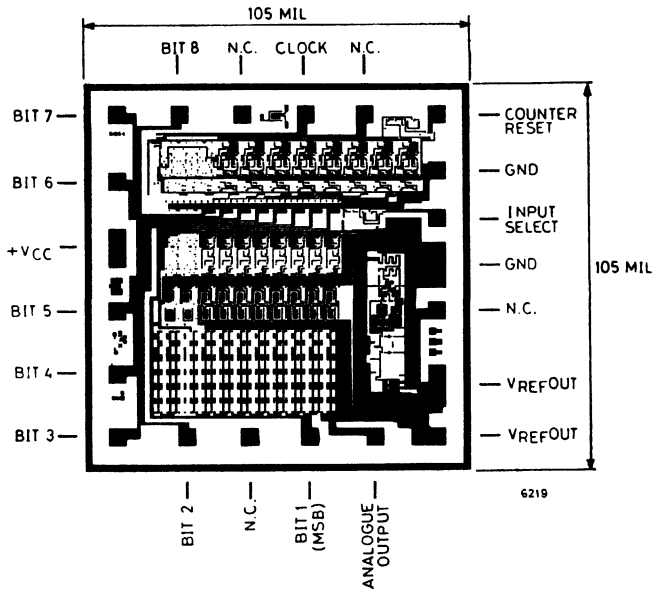
ZN426 Series

8 Bit Monolithic D to A Converter

FEATURES

- 8, 7 and 6-bit Accuracy
- ZN426E Series   Commercial Temp. Range   0°C to +70°C
- ZN426J-8   Military Temp. Range   −55°C to +125°C
- TTL and 5V CMOS Compatible
- Single +5V Supply
- Settling Time 1 μsec. Typical
- Only Reference Capacitor and Resistor required

DESCRIPTION

The ZN426 is a monolithic 8-bit digital to analogue converter containing an R-2R ladder network of diffused resistors with precision bipolar switches and a 2.5V precision voltage reference.
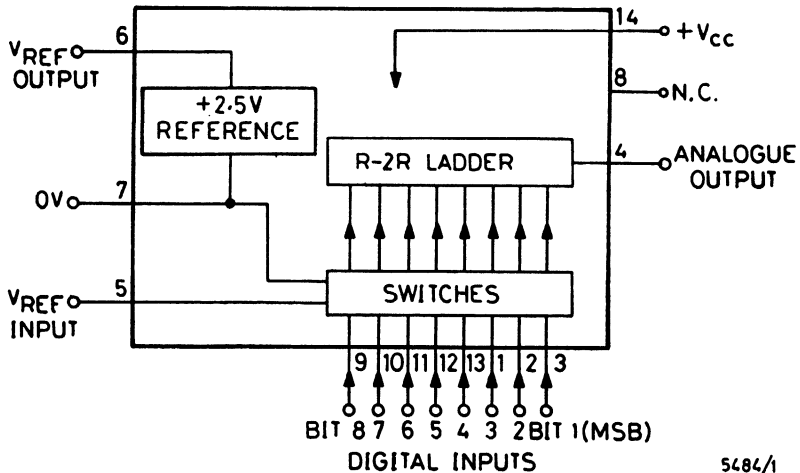
Fig. 1. System Diagram

ZN426 Series

INTRODUCTION

The ZN426 is an 8-bit digital to analogue converter. It contains an advanced design of R-2R ladder network and an array of precision bipolar switches plus a 2.5 volt precision voltage reference all on a single monolithic chip.

The special design of ladder network results in full 8-bit accuracy using normal diffused resistors.

The use of the on-chip reference voltage is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted. In this case there is no need to supply power to the internal reference so R_{REF} and C_{REF} can be omitted.

The converter is of the voltage switching type and uses an R-2R resistor ladder network as shown in Fig. 2.

Fig. 2. The R-2R Ladder Network

Each 2R element is connected either to 0V or V_{REF} by transistor switches specially designed for low offset voltage (typically 1 millivolt).

Binary weighted voltages are produced at the output of the R-2R ladder. the value depending on the digital number applied to the bit inputs.

ORDERING INFORMATION

Operating Temperature	8-bit accuracy	7-bit accuracy	6-bit accuracy	Package
0 to +70°C	ZN426E-8	ZN426E-7	ZN426E-6	Plastic
−55 to +125°C	ZN426J-8	—	—	Ceramic

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC} .. .. +7.0 volts

Max. voltage, logic and V_{REF} inputs .. .. +5.5 volts

Storage temperature range .. .. −55 to +125°C

ZN426 Series

ELECTRICAL CHARACTERISTICS ($V_{cc} = +5$ volts, $T_{amb} = 25°C$ unless otherwise specified).

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Converter Resolution		8	—	—	bits	
Accuracy (useful resolution) ZN426J-8⎤ ZN426E-8⎦ ZN426E-7 ZN426E-6		8 7 6	— — —	— — —	bits bits bits	V_{REF} input =2.0 to 3.0 volts
Non-linearity		—	—	±0.5	L.S.B.	*Note 1*
Differential non-linearity		—	±0.5	—	L.S.B.	*Note 2*
Settling time to 0.5 L.S.B.		—	1.0	—	µs	1 L.S.B. step
Settling time to 0.5 L.S.B.		—	2.0	—	µs	All bits ON to OFF or OFF to ON
Offset voltage ZN426J-8 ZN426E-8⎤ ZN426E-7 ⎬ ZN426E-6⎦	V_{OS}	— —	5.0 3.0	8.0 5.0	mV mV	All bits OFF *Note 1*
V_{OS} temperature coefficient		—	5	—	µV/°C	
Full scale output		2.545	2.550	2.555	volts	All bits ON Ext. V_{REF} = 2.560V
Full scale temp. coefficient		—	3	—	ppm/°C	Ext. V_{REF} = 2.560V
Non-linearity temp. coeff.		—	7.5	—	ppm/°C	Relative to F.S.R.

Notes:

1. The ZN426J-8 differs from the ZN426E-8 in the following respects:
   (a) For the ZN426J-8, the maximum linearity error may increase to ±0.4% FSR i.e. ±1 LSB over the temperature ranges −55°C to 0°C and +70°C to +125°C.
   (b) Offset voltage. The difference is due to package lead resistance. This offset will normally be removed by the setting up procedure, and because the offset temperature coefficient is low, the specified accuracy will be maintained.

2. Monotonic over full temperature range at resolution appropriate to accuracy.

ZN426 Series

ELECTRICAL CHARACTERISTICS *(continued)*

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Analogue output resistance	R_o	—	10	—	kΩ	
External reference voltage		0	—	3.0	volts	
Supply voltage	V_{CC}	4.5	—	5.5	Volts	
Supply current	I_s	—	5	9	mA	
High level input voltage	V_{IH}	2.0	—	—	volts	
Low level input voltage	V_{IL}	—	—	0.7	volts	
High level input current	I_{IH}	—	—	10	μA	V_{CC} = max., V_I = 2.4V
		—	—	100	μA	V_{CC} = max., V_I = 5.5V
Low level input current	I_{IL}	—	—	–0.18	mA	V_{CC} = max., V_I = 0.3V
Internal Voltage Reference Output voltage	V_{REF}	2.475	2.55	2.625	volts	*Note* * R_{REF} = 390Ω
Slope resistance	R_s	—	1	2	ohms	R_{REF} = 390Ω
V_{REF} temperature coefficient		—	40	—	ppm/°C	R_{REF} = 390Ω

Note * The internal reference requires a 1 μF stabilising capacitor between pins 7 and 6 (C_{REF}) and a 390Ω resistor between pins 14 and 6 (R_{REF}).

APPLICATIONS

1. 8-bit D to A Converter

The ZN426 gives an analogue voltage output directly from pin 4 therefore the usual current to voltage converting amplifier is not required. The output voltage drift, due to the temperature coefficient of the Analogue Output Resistance R_o, will be less than 0.004% per °C (or 1 L.S.B./100°C) if R_L is chosen to be $\geqslant$ 650 kΩ

In order to remove the offset voltage and to calibrate the converter a buffer amplifier is necessary. Fig. 3 shows a typical scheme using the internal reference voltage. To minimise temperature drift in this and similar applications the source resistance to the inverting input of the operational amplifier should be approximately 6 kΩ. The calibration procedure is as follows:

i. Set all bits to OFF (low) and adjust R_2 until V_{out} = 0.000V.

ii. Set all bits to ON (high) and adjust R_1 until V_{out} = Nominal full scale reading –1 L.S.B.

iii. Repeat *i.* and *ii.*

e.g. Set F.S.R. to +3·840 volts – 1 L.S.B. = 3·825 volts

$$(1 \text{ L.S.B.} = \frac{3 \cdot 84}{256} = 15.0 \text{ millivolts.})$$

42

Fig. 3. 8-bit Digital to Analogue Converter

Alternative Output Buffer using the ZLD741

The following circuit, employing the ZLD741 operational amplifier, may be used as the output buffer (Fig. 3).
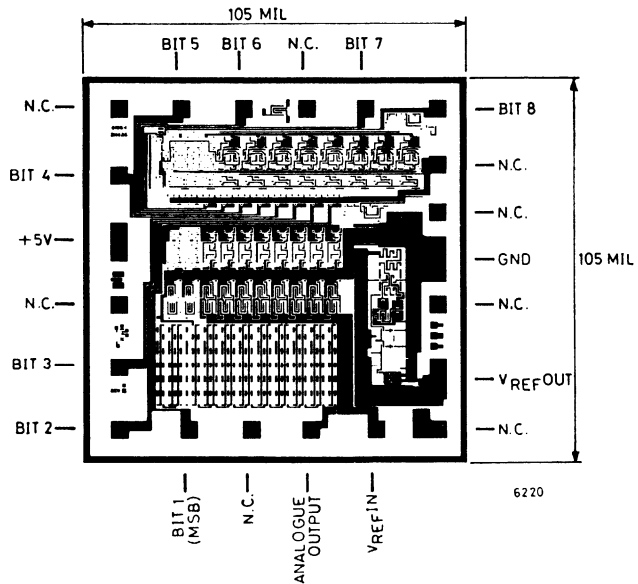

Fig. 4. The ZLD741 as Output Buffer

43

ZN426 Series

Bit 3	1	14 +V$_{CC}$ (+5 volts)
Bit 2	2	13 Bit 4
(MSB) Bit 1	3	12 Bit 5
Analogue Output	4	11 Bit 6
V$_{REF}$ IN	5	10 Bit 7
V$_{REF}$ OUT	6	9 Bit 8 (LSB)
0V	7	8 N.C.

5798

CHIP DIMENSIONS AND LAYOUT

105 MIL

BIT 5   BIT 6   N.C.   BIT 7

N.C. — — BIT 8

BIT 4 — — N.C.

+5V — — N.C.

— GND   105 MIL

N.C. — — N.C.

BIT 3 — — V$_{REF}$ OUT

BIT 2 — — N.C.

BIT 1 (MSB)   N.C.   ANALOGUE OUTPUT   V$_{REF}$ IN

6220

44

FERRANTI semiconductors

ZN427E-8
ZN427J-8

8 Bit Successive Approximation A/D Converter

FEATURES

● Fast; 10 μs conversion time guaranteed
● 3-state outputs, TTL compatible
● Internal or external reference
● No missing codes over operating temperature range
● Unipolar and bipolar input ranges
● Ratiometric conversion
● +5V and −3V to −30V supplies
● ZN427E-8   Commercial temp. range   0°C to +70°C
● ZN427J-8   Military temp. range   −55°C to +125°C

DESCRIPTION

The ZN427 is an 8-bit A to D converter with 3-state outputs to permit bussing on common data lines. It contains a voltage switching D to A converter, a 2.5 volts precision reference, a fast comparator and successive approximation logic.

The use of the on-chip reference voltage is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted.

Only passive external components are required. For basic operation these are an input resistor, a reference resistor and capacitor and a resistor from R_{EXT} (pin 5) to the negative rail (V_-).
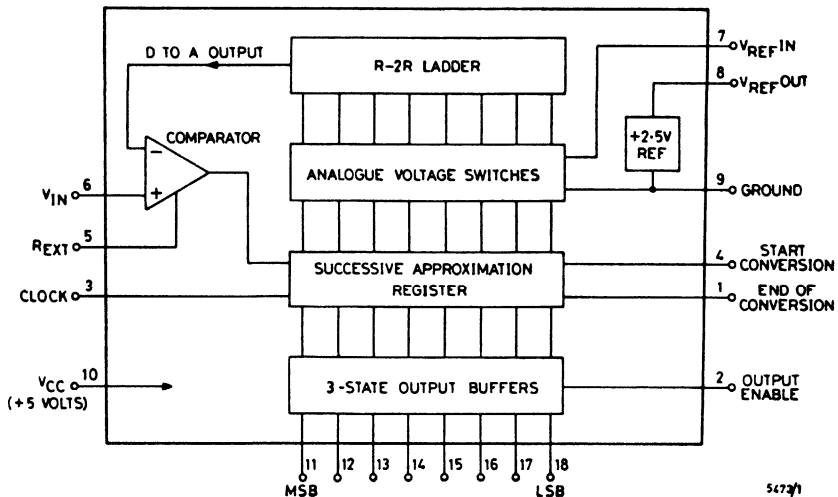
Fig. 1. SYSTEM DIAGRAM

ZN427E-8/J-8

ABSOLUTE MAXIMUM RATINGS
Supply Voltage, V_{CC} .. .. $+7.0$ volts
Max. Voltage, Logic and V_{REF} inputs .. .. V_{CC}
Operating temperature range .. .. $0°C$ to $+70°C$ (ZN427E-8)
                                                    $-55°C$ to $+125°C$ (ZN427J-8)
Storage temperature range .. .. $-55°C$ to $+125°C$

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_{amb} = 25°C$ unless otherwise specified).

	Min.	Typ.	Max.	Units	Conditions
Internal Voltage Reference					
Output Voltage	2.475	2.550	2.625	V	$R_{REF} = 390\Omega$
					$C_{REF} = 1\ \mu F$
Slope Resistance		0.5	2	Ω	
V_{REF} Temperature Coefficient		50		ppm/°C	
Reference Current	4		15	mA	See REFERENCE Page 4
Comparator					
Input Current		1		μA	$\{V_{IN} = 3V, R_{EXT} = 82k\Omega$
Input Impedance		100		$k\Omega$	$\{V_- = -5V$
Tail Current, I_{EXT}	25		150	μA	
Negative Supply, V_-	-3.0		-30.0	V	See COMPARATOR
Input Voltage	-0.5		3.5	V	Page 51
Converter					
Linearity Error			± 0.5	LSB	
Differential Non-Linearity		± 0.5		LSB	
Linearity Error T.C.		± 3		ppm/°C	
Differential Non-Linearity T.C.		± 6		ppm/°C	
Full Scale (Gain) T.C.		± 2.5		ppm/°C	External Ref. 2.5V
Zero T.C.		± 8		$\mu V/°C$	
Zero Transition 00000000→ 00000001	12	15	18	mV	$V_{REF\ IN} = 2.560V$
F.S. Transition 11111110→ 11111111	2.545	2.550	2.555	V	$V_{REF\ IN} = 2.560V$
Conversion Time		10	15	μs	
External Reference Voltage	1.5		3.0	V	
Supply Voltage (V_{CC})	4.5		5.5	V	
Supply Current		25	40	mA	
Power Consumption		125		mW	
Logic (over operating temp.)					
High Level Input Voltage	2			V	
Low Level Input Voltage			0.8	V	
High Level Input Current			50	μA	$V_{IN} = 5.5V$, V_{CC} = max.
			15	μA	$V_{IN} = 2.4V$, V_{CC} = max.
High Level Input Current			100	μA	$V_{IN} = 5.5V$, V_{CC} = max.
Clock Input			30	μA	$V_{IN} = 2.4V$, V_{CC} = max.
Low Level Input Current			-5	μA	$V_{IN} = 0.4V$, V_{CC} = max.
High Level Output Current I_{OH}			-100	μA	
Low Level Output Current I_{OL}			1.6	mA	
High Level Output Voltage	2.4			V	I_{OH} = max., V_{CC} = min.
Low Level Output Voltage			0.4	V	I_{OL} = max., V_{CC} = min.
Disabled Output Leakage			2	μA	$V_O = 2.4V$
Max. Clock Frequency	900	1000		kHz	Note below
Clock Pulse Width	500			ns	
Enable/Disable Delay Time		180	250	ns	See Fig. 10
Duration of Start Conversion(SC) Pulse	250	160		ns	
Input Clamp Diode Voltage		-1.5		V	$I_{IN} = -8\,mA$

Note: 900 KHz clock corresponds to a conversion time of 10 μs (nine clock periods).

48

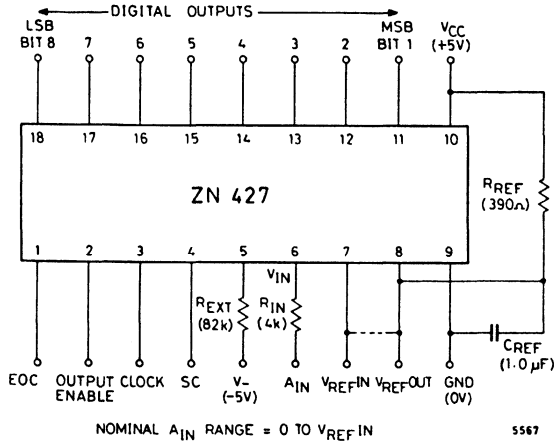NOMINAL A_{IN} RANGE = 0 TO V_{REF} IN

5567

Fig. 2. EXTERNAL COMPONENTS FOR BASIC OPERATION

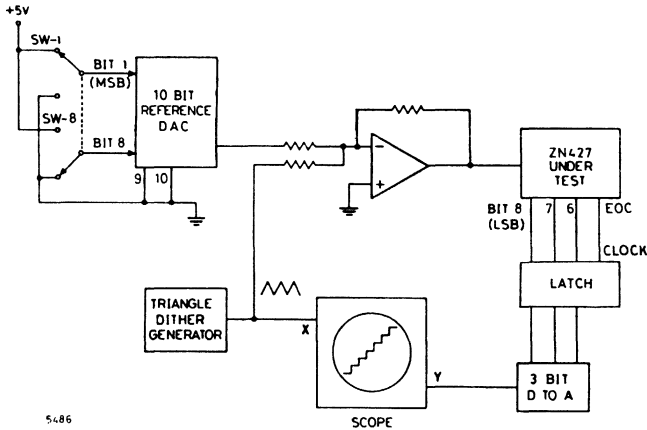## TEST CIRCUIT

5486

SCOPE

Fig. 3. DYNAMIC CROSSPLOT ACCURACY TEST

Switches SW-1 to SW-8 are set to the appropriate digital code to select the point on the characteristic to be displayed. For example, code 1000 0000 would select half full scale, i.e. the major transition.

The output from the dither generator (suggested peak to peak amplitude = $\pm 4 \times$ LSB) is used as the X deflection for the scope and is also superimposed on the analogue output from the reference D.A.C. in the summing amplifier. The resulting analogue signal including dither is used as V_{IN} for the ZN427 under test.

Bit 8, 7 and 6 outputs are fed to the inputs of a 3 bit D.A.C. of at least 6 bit accuracy and the analogue output used as the Y deflection for the scope. Differential non-linearity is shown by horizontal lines which are longer or shorter than the rest.

49

ZN427E-8/J-8

GENERAL CIRCUIT GUIDELINES

OPERATION

At the start of conversion the MSB is set to a 1 and all the other bits are set to 0. This produces a voltage output from the D to A converter of $\frac{1}{2}(V_{REF\ IN})$. This value is compared with the input voltage, V_{IN} and a decision is made on the first (negative) clock edge to set the MSB to 0 if $\frac{1}{2}(V_{REF\ IN}) > V_{IN}$ or retain a 1. Bit 2 is switched to a 1 on the same clock edge and on the next edge a decision is made regarding Bit 2, again by comparing the D to A output with V_{IN}. This process is repeated for all eight bits so that when the End of Conversion (EOC) output goes HIGH the digital output from the converter is a valid representation of V_{IN}. The binary output data is latched until the next Start Conversion (SC) pulse.

Detailed waveforms are shown in the Timing Diagram (Fig. 11).

D to A CONVERTER

The converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig. 4. Each 2R element is connected either to 0V or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (<1 millivolt).

A binary weighted voltage is produced at the output of the R-2R ladder:

$$D \text{ to A Output} = \frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$$

where n is the digital input to the D to A from the successive approximation register.

V_{OS} is a small offset voltage that is produced by the device supply current flowing in the package lead resistance. The value of V_{OS} is typically 2 mV for the ZN427E-8 (4 mV, ZN427J-8). This offset will normally be removed by the setting up procedure and since the offset temperature coefficient is low (8 μV/°C) the effect on accuracy will be negligible.

The D to A output range can be considered to be $0-V_{REF\ IN}$ through an output resistance R (4kΩ).
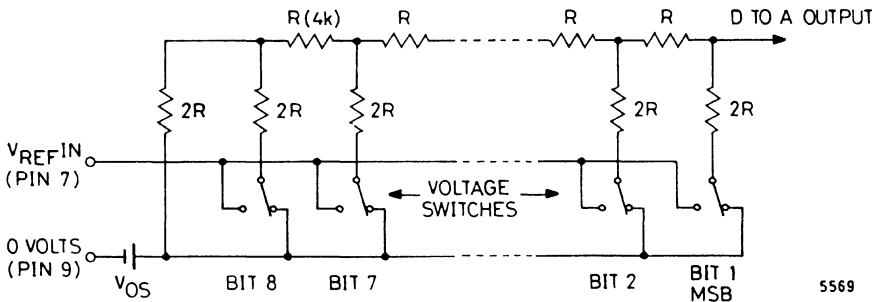
Fig. 4. R-2R LADDER NETWORK

REFERENCE

(a) Internal Reference

The internal reference is an active band gap circuit which is equivalent to a 2.5V Zener diode with a very low slope impedance (Fig. 5). A resistor (R_{REF}) should be connected between pins 8 and 10. The recommended value of 390Ω will supply a nominal reference current of $(5.0 - 2.5)/0.39 = 6.4$ mA. A stabilising/decoupling capacitor, C_{REF} (1 μF), is required between Pins 8 and 9. For internal reference operation $V_{REF\ OUT}$ (Pin 8) is connected to $V_{REF\ IN}$ (Pin 7).

Up to five ZN427s may be driven from one internal reference, there being no need to reduce R_{REF}. This useful feature saves power and gives excellent gain tracking between the converters.
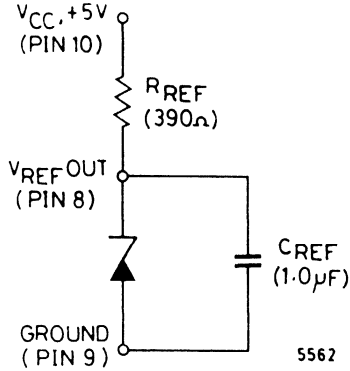
Fig. 5. INTERNAL VOLTAGE REFERENCE

(b) **External Reference**

If required an external reference voltage in the range $+1.5$ to $+3.0$ volts may be connected to $V_{REF\ IN}$. The slope resistance of such a reference source should be less than $\dfrac{2.5\Omega}{n}$, where n is the number of converters supplied.

COMPARATOR

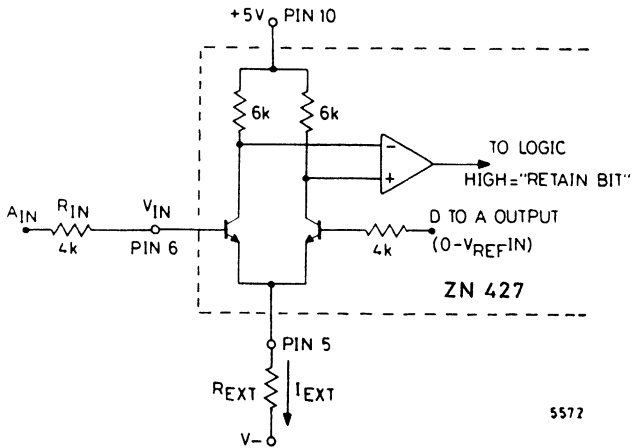The ZN427 contains a fast comparator, the equivalent input circuit of which is shown in **Fig. 6.**

Fig. 6. COMPARATOR EQUIVALENT CIRCUIT

ZN427E-8/J-8

The comparator derives the tail current, I_{EXT}, for its first stage from an external resistor, R_{EXT}, which is taken to a negative supply V_-.

This arrangement allows the ZN427 to work with any negative supply in the range –3 to –30 volts. The ZN427 is designed to be insensitive to changes in I_{EXT} from 25 μA to 150 μA. The suggested nominal value of I_{EXT} is 65 μA and a suitable value for R_{EXT} is given by $R_{EXT} = |V_-| \, 15 \, k\Omega$.

V_- Volts	R_{EXT} ($\pm 10\%$)
–3	47 kΩ
–5	82 kΩ
–10	150 kΩ
–12	180 kΩ
–15	220 kΩ
–20	330 kΩ
–25	390 kΩ
–30	470 kΩ

The output from the D to A converter is connected through the 4 kΩ ladder resistance to one side of the comparator. The analogue input to be converted could be connected directly to the other comparator input (V_{IN}, Pin 6) but for optimum stability with temperature the analogue input should be applied through a source resistance ($R_{IN} = 4 \, k\Omega$) to match the ladder resistance.

ANALOGUE INPUT RANGES

The basic input range of the ZN427 is 0 to $V_{REF \, IN}$. Other input ranges, e.g. $+5V$, $+10V$, $\pm 5V$ and $\pm 10V$ can be readily obtained by using different setting up resistors (see APPLICATIONS).

LOGIC INPUTS AND OUTPUTS

Equivalent circuits for the logic inputs and outputs are shown in figures 7, 8 and 9. The 3-state data outputs are OFF (high impedance) when Output Enable is LOW. If EOC is connected to Output Enable the data outputs will automatically be enabled when valid.

5561
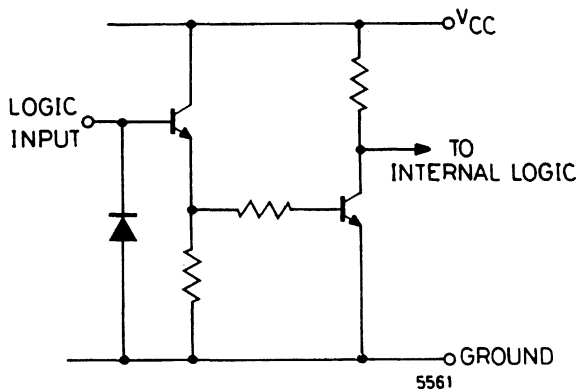
Fig. 7. EQUIVALENT CIRCUIT OF ALL INPUTS

52
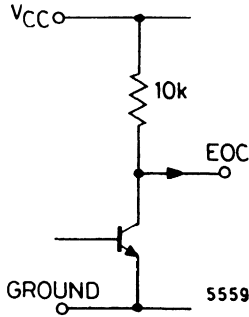
Fig. 8. EQUIVALENT CIRCUIT OF EOC OUTPUT
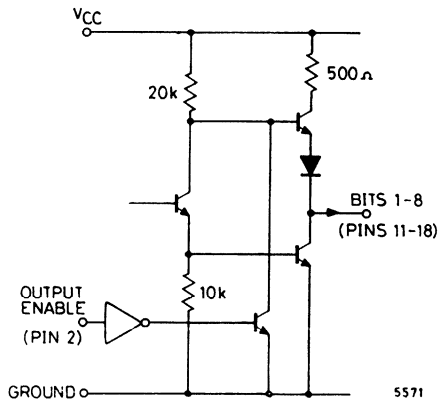
Fig. 9. EQUIVALENT CIRCUIT OF DATA OUTPUTS

T_E = ENABLE DELAY TIME (C_L = 50pF)

T_D = DISABLE DELAY TIME (C_L = 10pF)
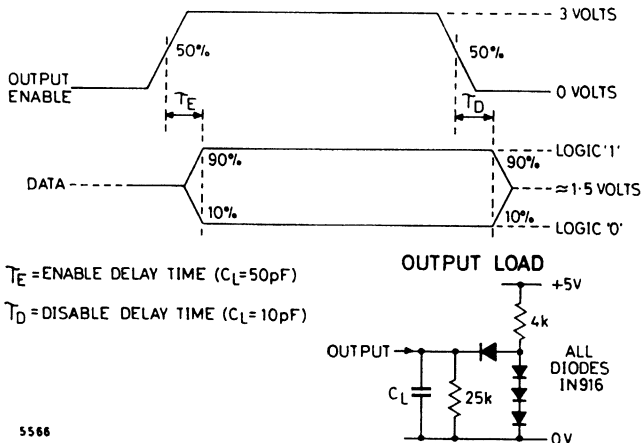
Fig. 10. OUTPUT ENABLE/DISABLE WAVEFORMS

ZN427E-8/J-8

CONVERSION TIMING DETAILS
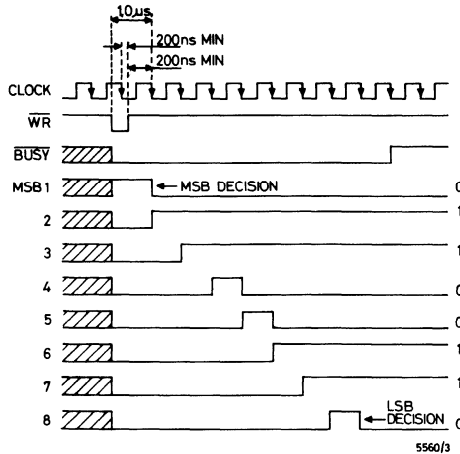
Fig. 11. TIMING DIAGRAM

Notes on Timing Diagram

1. Conversion is initiated by a Start Conversion (SC) pulse which sets the MSB to 1 and all other bits to 0.

2. To allow for MSB settling, the first active (negative going) edge of Clock pulse after the SC pulse should not occur until at least 1.0 μs after the negative edge of the SC pulse.

3. The positive edge of the SC pulse should not occur within 200 ns of an active clock edge.

4. As a special case of conditions (2) and (3) the SC pulse may be coincident with and of the same duration as a negative going clock pulse.

5. Cross hatching indicates a 'don't care' condition.

6. The output data is valid when End of Conversion (EOC) goes HIGH and remains latched until the next SC pulse.

7. The conversion sequence shown is for the digital word 01100110. For clarity the digital outputs are shown enabled during the conversion. Normally the outputs will be disabled during conversion and enabled after EOC goes HIGH.

APPLICATIONS

1. Unipolar Operation

The basic connection of the ZN427 (Fig. 2) will accept an input signal from 0 to $V_{REF\ IN}$ which in some applications can be made directly available from previous conditioning/scaling amplifiers.

Other input ranges can be obtained by connecting a simple resistor network to V_{IN} (Pin 6) as shown in Fig. 12. The values of R_1 and R_2 are chosen so that $V_{IN} = V_{REF\ IN}$ when the Analogue Input (A_{IN}) is at full scale. The resulting full scale range is given by

$$A_{IN}\ FS = (1 + \frac{R1}{R2}) \cdot V_{REF\ IN} = G \cdot V_{REF\ IN}.$$

To match the ladder resistance $R_1 // R_2\ (\approx R_{IN}) = 4$ kΩ.

The required nominal values of R_1 and R_2 are given by $R_1 = 4G$ kΩ, $R_2 = \frac{4G}{G-1}$ kΩ.

54
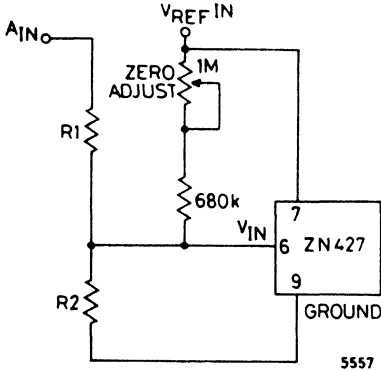
Fig. 12. UNIPOLAR OPERATION – GENERAL CONNECTION

Using these relationships a table of nominal values of R_1 and R_2 can be constructed for $V_{REF\ IN}$ = 2.5 volts.

Input Range	G	R_1	R_2
+5V	2	8 kΩ	8 kΩ
+10V	4	16 kΩ	5.33 kΩ

For gain setting R_1 is adjusted about its nominal value. Components for zero adjust are as shown (G ⩾ 1.5).

Practical circuit realisations for +5V and +10V input ranges are given in Fig. 13.

± 2% RESISTORS
± 20% POTENTIOMETERS
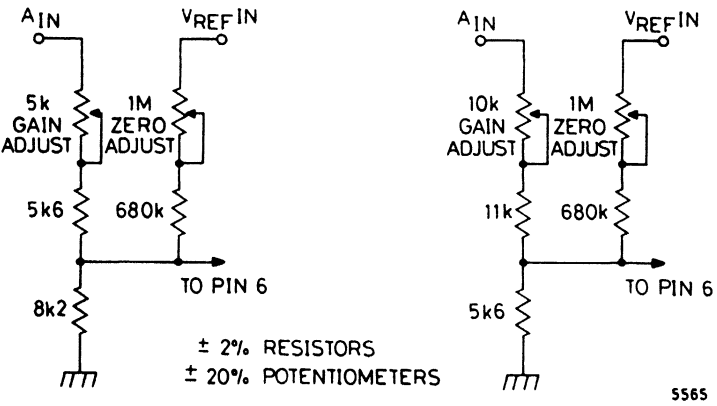
+ 5 VOLTS FULL SCALE   + 10 VOLTS FULL SCALE

Fig. 13. UNIPOLAR OPERATION – COMPONENT VALUES

Unipolar Adjustment Procedure

(i) Apply continuous SC pulses at intervals long enough to allow a complete conversion and monitor the digital outputs.

(ii) Apply full scale minus $1\frac{1}{2}$ LSB to A_{IN} and adjust gain until Bit 8 (LSB) output just flickers between 0 and 1 with all other bits at 1.

(iii) Apply $\frac{1}{2}$ LSB to A_{IN} and adjust zero until Bit 8 just flickers between 0 and 1 with all other bits at 0.

UNIPOLAR SETTING-UP POINTS

Input Range, +FS	$\frac{1}{2}$ LSB	FS $-1\frac{1}{2}$ LSB
+5V	9.8 mV	4.9707 volts
+10V	19.5 mV	9.9414 volts

$$1 \text{ LSB} = \frac{FS}{256}$$

UNIPOLAR LOGIC CODING

Analogue Input (A_{IN}) (Nominal code centre value)	Output Code (Binary)
FS -1 LSB	11111111
FS -2 LSB	11111110
$\frac{3}{4}$ FS	11000000
$\frac{1}{2}$ FS $+ 1$ LSB	10000001
$\frac{1}{2}$ FS	10000000
$\frac{1}{2}$ FS $- 1$ LSB	01111111
$\frac{1}{4}$ FS	01000000
1 LSB	00000001
0	00000000

2. Bipolar Operation

For bipolar operation the input to the ZN427 is offset by half full scale by connecting a resistor R_3 between $V_{REF\ IN}$ and V_{IN} (Fig. 14).
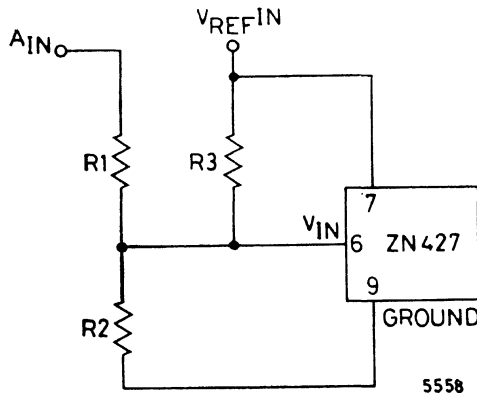
Fig. 14. BIPOLAR OPERATION – GENERAL CONNECTION

When $A_{IN} = -FS$, V_{IN} needs to be equal to zero.

When $A_{IN} = +FS$, V_{IN} needs to be equal to $V_{REF\ IN}$.

If the full scale range is $\pm G$. $V_{REF\ IN}$ then $R_1 = (G-1)$. R_2 and $R_1 = G$. R_3 fulfil the required conditions.

To match the ladder resistance $R_1//R_2//R_3$ $(= R_{IN}) = 4\ k\Omega$.

Thus the nominal values of R_1, R_2, R_3 are given by $R_1 = 8\ G k\Omega$, $R_2 = 8G/(G-1)k\Omega$, $R_3 = 8\ k\Omega$.

A bipolar input range of $\pm V_{REF\ IN}$ (which corresponds to the basic unipolar range 0 to $+V_{REF\ IN}$) results if $R_1 = R_3 = 8\ k\Omega$ and $R_2 = \infty$.

Assuming that $V_{REF\ IN} = 2.5$ volts the nominal values of resistors for $\pm 5V$ and $\pm 10V$ input ranges are given in the following table.

Input Range	G	R_1	R_2	R_3
$\pm 5V$	2	16 kΩ	16 kΩ	8 kΩ
$\pm 10V$	4	32 kΩ	10.66 kΩ	8 kΩ

Minus full scale (offset) is set by adjusting R_1 about its nominal value relative to R_3. Plus full scale (gain) is set by adjusting R_2 relative to R_1.

Practical circuit realisations are given in Fig. 15.
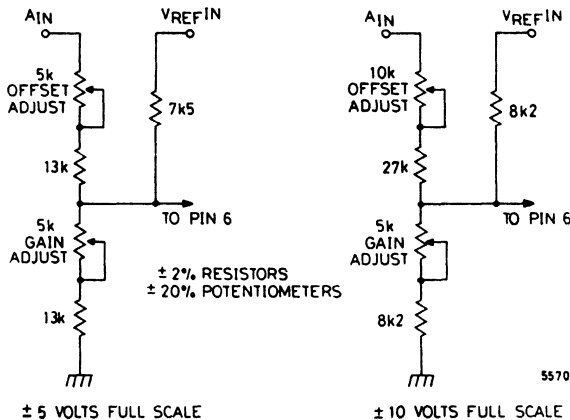
Fig. 15. BIPOLAR OPERATION – COMPONENT VALUES

Note that in the $\pm 5V$ case R_3 has been chosen as 7.5 kΩ (instead of 8.2 kΩ) to get a more symmetrical range of adjustment using standard potentiometers.

Bipolar Adjustment Procedure

(i) Apply continuous SC pulses at intervals long enough to allow a complete conversion and monitor the digital outputs.

(ii) Apply $-(FS - \frac{1}{2} LSB)$ to A_{IN} and adjust offset until the Bit 8 (LSB) output just flickers between 0 and 1 with all other bits at 0.

(iii) Apply $+ (FS - 1\frac{1}{2} LSB)$ to A_{IN} and adjust gain until Bit 8 just flickers between 0 and 1 with all other bits at 1.

(iv) Repeat step (ii).

ZN427E-8/J-8

BIPOLAR SETTING-UP POINTS

Input Range, $\pm$FS	$-(FS - \frac{1}{2} LSB)$	$+(FS - 1\frac{1}{2} LSB)$
$\pm$5V	$-4.9805V$	$+4.9414V$
$\pm$10V	$-9.9609V$	$+9.8828V$

$$1 \text{ LSB} = \frac{2FS}{256}$$

BIPOLAR LOGIC CODING

Analogue Input (A_{IN}) (Nominal code centre value)	Output Code (Offset Binary)
$+(FS - 1 \text{ LSB})$	11111111
$+(FS - 2 \text{ LSB})$	11111110
$+\frac{1}{2}FS$	11000000
$+1 \text{ LSB}$	10000001
0	10000000
-1 LSB	01111111
$-\frac{1}{2}FS$	01000000
$-(FS - 1 \text{ LSB})$	00000001
$-FS$	00000000

3. Single 5 Volt Supply Rail Operation

The ZN427 takes very little power from the negative rail and so a suitable negative supply can be generated very easily using a 'diode pump' circuit. The circuit shown in Fig. 16 works with any clock frequency from 10 kHz to 1 MHz and can supply up to five ZN427s.
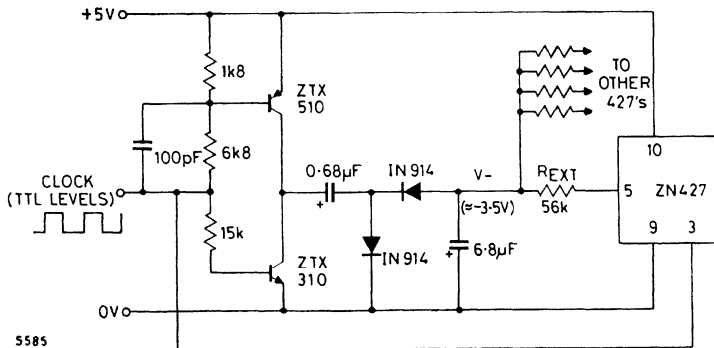
Fig. 16. SINGLE 5 VOLT SUPPLY OPERATION

4. Ratiometric Operation

If the output from a transducer varies with its supply then an external reference for the ZN427 should be derived from the same supply. The external reference can vary from +1.5 volts to +3.0 volts. The ZN427 will still operate if $V_{REF\ IN}$ is less than +1.5 volts but reduced overdrive to the comparator will increase its delay and so the conversion time will need to be increased.

58

ZN427E-8/J-8

PIN CONNECTIONS

END OF CONVERSION 1	18 Bit 8(LSB)
OUTPUT ENABLE 2	17 Bit 7
CLOCK 3	16 Bit 6
START CONVERSION 4	15 Bit 5
R_{EXT} 5	14 Bit 4
V_{IN} 6	13 Bit 3
$V_{REF IN}$ 7	12 Bit 2
$V_{REF OUT}$ 8	11 Bit 1(MSB)
GROUND 9	10 +V_{cc}(+5volts)

5832

CHIP DIMENSIONS AND LAYOUT

92 MIL

124 MIL

OUTPUT ENABLE — ECC — GND — BIT 8 — BIT 7

CLOCK —
SC —
R_{EXT} —
V_{IN} —
V_{REF} IN —

— BIT 6
— BIT 5
— BIT 4
— BIT 3
— BIT 2

V_{REF} OUT — GND — GND — BIT 1 (MSB)

6221

59

FERRANTI semiconductors
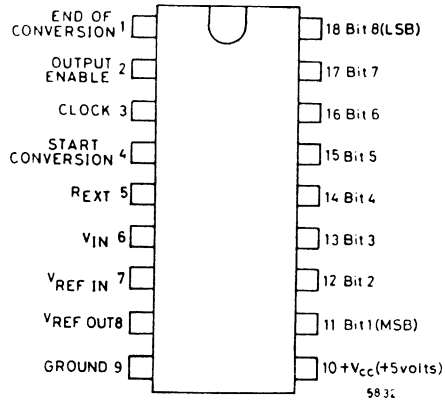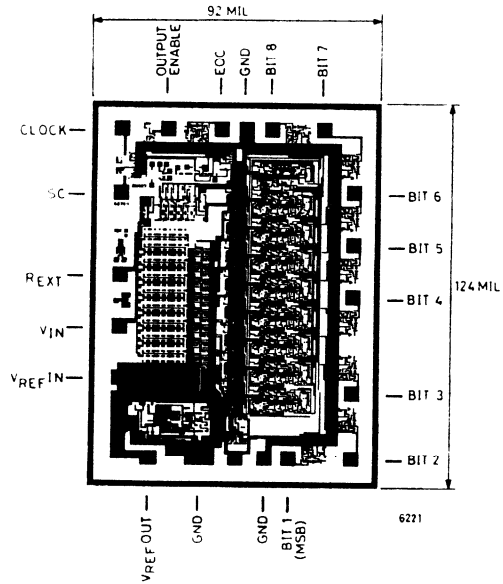
8 Bit Latched Input Monolithic D to A Converter

FEATURES

● Contains DAC with data latch and on-chip reference.

● Guaranteed monotonic over the full operating temperature range

● Single +5V supply

● TTL and 5V CMOS compatible

● 800 ns settling time

● ZN428E-8   Commercial temperature range   0˚C to +70˚C

● ZN428J-8   Military temperature range   −55˚C to +125˚C

GENERAL DESCRIPTION

The ZN428 is a Monolithic 8 bit D to A converter with input latches to facilitate up-dating from a data bus. The latch is transparent when Enable is LOW and the data is held when Enable is taken HIGH. The ZN428 also contains a 2.5 volt reference the use of which is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted.

Fig. 1 SYSTEM DIAGRAM

61
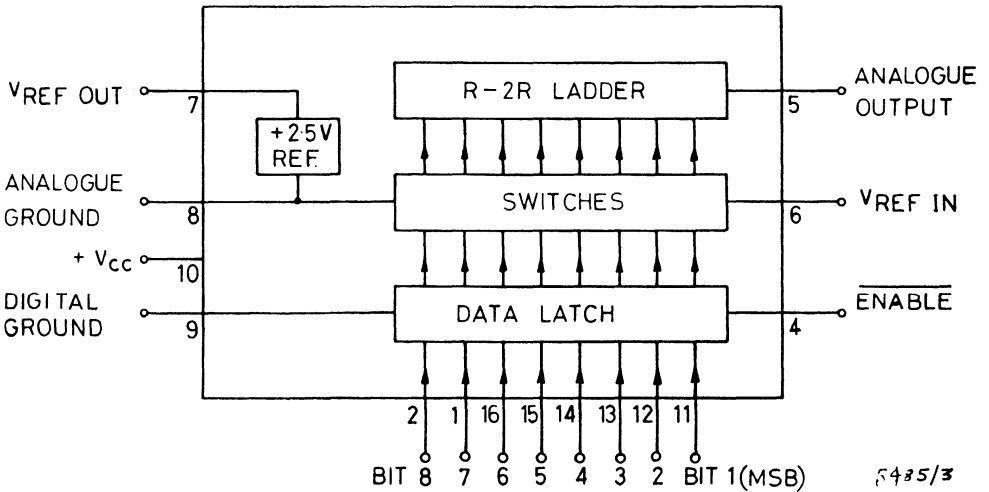
ZN428E-8/J-8

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC} .. .. +7.0 volts

Max. voltage, logic and V_{REF} input .. .. $+V_{CC}$

Operating temperature range .. .. 0°C to +70°C (ZN428E-8)
$\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad$ −55°C to +125°C (ZN428J-8)

Storage temperature range .. .. −55°C to +125°C

Analogue Ground to Digital Ground .. .. ±200 mV

ELECTRICAL CHARACTERISTICS (V_{CC} = +5 volts, T_{amb} = 25°C unless otherwise specified).

Parameter	Min.	Typ.	Max.	Units	Conditions
Internal Voltage Reference					
Output voltage	2.475	2.550	2.625	volts	$R_{REF} = 390\,\Omega$
Slope resistance		0.5	2	Ω	$C_{REF} = 1\ \mu F$
$V_{REF\,OUT}$ T.C.		50		ppm/°C	
Reference current	4		15	mA	Note 1
D to A Converter Linearity error			±0.5	LSB	2.0V $\leqslant V_{REF\,IN} \leqslant$ 3.0V
Differential non-linearity		±0.5		LSB	
Linearity error T.C.		±3		ppm/°C	
Differential non-linearity T.C.		±6		ppm/°C	
Offset voltage		2	5	mV	All bits OFF
Offset voltage T.C.		±6		µV/°C	
Full scale output	2.545	2.550	2.555		External reference
Full scale output T.C.		2		ppm/°C	$V_{REF\,IN}$ = 2.560 volts, all bits ON
Analogue output resistance		4		kΩ	
External reference voltage	0		3.0	volts	
Settling time to 0.5 LSB		800		ns	1 LSB Major Transition (Note 2)
		1.25		µs	All bits ON to OFF or OFF to ON (Note 2)
Operating temperature range : ZN428E-8	0		70	C	
ZN428J-8	−55		125	C	
Supply voltage (V_{CC})	4.5	5.0	5.5	volts	

Note 1 See REFERENCE, page 64.
Note 2 R_L = 10 MΩ, C_L = 10 pF.

ZN428E-8/J-8

ELECTRICAL CHARACTERISTICS *(continued)*

	Min.	Typ.	Max.	Units	Conditions
Supply current		20	30	mA	Note 3
Power consumption		100		mW	
Logic (over specified operating temperature range) High level input voltage	2.0			V	
Low level input voltage			0.8	V	
High level input current			60	μA	$V_{IN} = 5.5V$ $V_{CC} = $ Max.
			20	μA	$V_{IN} = 2.4V$ $V_{CC} = $ Max.
Low level input current			−5	μA	$V_{IN} = 0.4V$ $V_{CC} = $ Max.
Input Clamp Diode Voltage		−1.5		V	$I_{IN} = -8$ mA
Enable pulse width	100			ns	
Data set-up time	150			ns	Note 4
Data hold time	10			ns	Note 5

Note 3 All inputs HIGH ($V_{IH} = 3.5$ volts).

Note 4 Set up time before $\overline{\text{Enable}}$ goes high.

Note 5 Hold time after $\overline{\text{Enable}}$ goes high.

D to A CONVERTER

The converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig. 2. Each 2R element is connected to 0V or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (<1 millivolt). A binary weighted voltage is produced at the output of the R-2R ladder.

Fig. 2. The R-2R Ladder Network

63
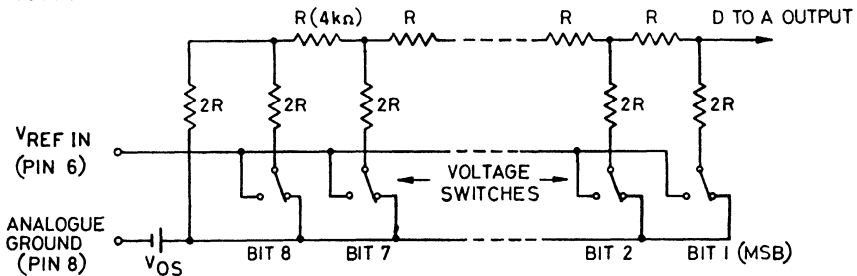
ZN428E-8/J-8

$$\text{Analogue Output} = \frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$$

where n is the digital input to the D to A from the data latch.

V_{OS} is a small offset voltage produced by the D to A switch currents flowing through the package lead resistance. The value of V_{OS} is tyically 1 mV. This offset will normally be removed by the setting up procedure (see APPLICATIONS section) and because the offset temperature coefficient is low (± 6 μV/°C) the effect on accuracy is negligible.
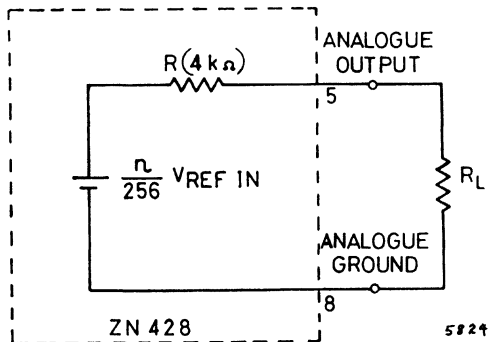
Fig. 3. Analogue Output Equivalent Circuit

Fig. 3 shows an equivalent circuit of the output (ignoring V_{OS}). The output resistance R has a temperature coefficient of $+0.2\%$ per °C.

The gain drift due to this is $\dfrac{0.2R}{R+R_L}$ % per °C

RL should be chosen to be as large as possible to make the gain drift small. As an example if $R_L = 400$ kΩ then the gain drift due to the T.C. of R for a 100°C change in ambient temperature will be less than 0.2%. Alternatively the ZN428 can be buffered by an amplifier (see APPLICATIONS section).

REFERENCE

(a) **Internal Reference**

The internal reference is an active band gap circuit which is equivalent to a 2.5 volt Zener diode with a very low slope impedance (Fig. 4). A resistor (R_{REF}), should be connected between $+V_{CC}$ (pin 10) and pin 7. The recommended value of 390Ω will supply a nominal reference current of $(5.0–2.5)/0.39 = 6.4$ mA. A stabilising/decoupling capacitor, $C_{REF} = 1$ μF is required between pins 7 and 8 for internal reference operation, $V_{REF\ OUT}$ (pin 7) being connected to $V_{REF\ IN}$ (pin 6).

Up to five ZN428s may be driven from one internal reference (there is no need to reduce R_{REF}) This useful feature saves power and gives excellent gain tracking between the converters.

(b) **External Reference**

If required an external reference voltage may be connected to $V_{REF\ IN}$. The slope resistance of such a reference source should be less than $\dfrac{2.5}{n}$ Ω, where n is the number of converters supplied.

$V_{REF\ IN}$ can be varied from 0 to $+3$ volts for ratiometric operation. The ZN428 is guaranteed monotonic for $V_{REF\ IN}$ above 2 volts.
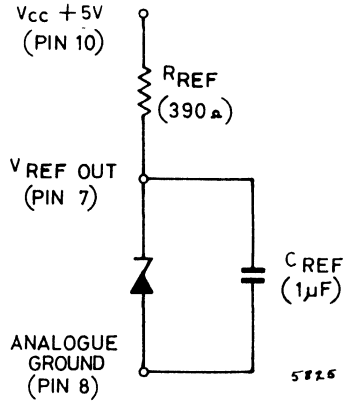
Fig. 4. Internal Voltage Reference

LOGIC

Input coding is binary for unipolar operation and offset binary for bipolar operation. When the Enable input is low the data inputs drive the D to A directly. When Enable goes high the input data word is held in the data latch.

The equivalent circuit for the data and clock inputs is shown in Fig. 5.

The ZN428 is provided with separate analogue and digital ground connections. The circuit will operate correctly with as much as ± 200 mV between the two grounds.
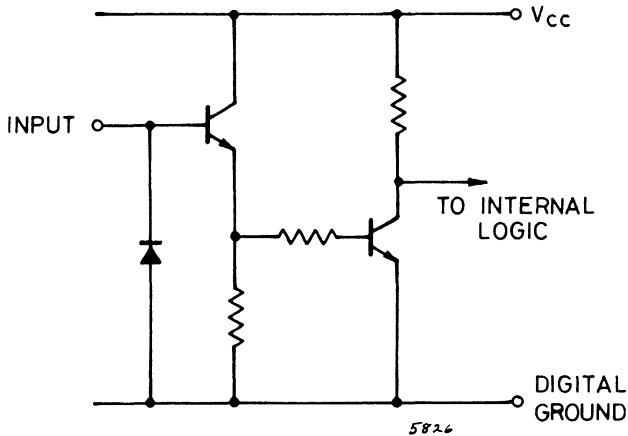
Fig. 5. Equivalent Circuit of All Inputs

65

ZN428E-8/J-8

APPLICATIONS

(1) Unipolar D to A Converter

The nominal output range of the ZN428 is 0 to $V_{REF\ IN}$ through a 4 kΩ resistance. Other output ranges can readily be obtained by using an external amplifier.

The general scheme (Fig. 6) is suitable for amplifiers with input bias currents less than 1.5 μA.

The resulting full scale range is given by

$$V_{OUT}\ FS = \left(1 + \frac{R1}{R2}\right) V_{REF\ IN} = G. V_{REF\ IN}$$

The impedance at the inverting input is R1//R2 and for low drift with temperature this parallel combination should be equal to the ladder resistance (4 kΩ). The required nominal values of R1 and R2 are given by R1 = 4G kΩ and R_2 = 4G/(G-1) kΩ.

Using these relationships a table of nominal resistance values for R_1 and R_2 can be constructed for $V_{REF\ IN}$ = 2.5 volts.

Output Range	G	R_1	R_2
+5V	2	8kΩ	8kΩ
+10V	4	16kΩ	5.33kΩ

For gain setting R_1 is adjusted about its nominal value. Practical circuit realisations (including amplifier stabilising components) for +5V and +10V output ranges are given in Fig. 7. Settling time for a major transition is 1.5 μs typical.
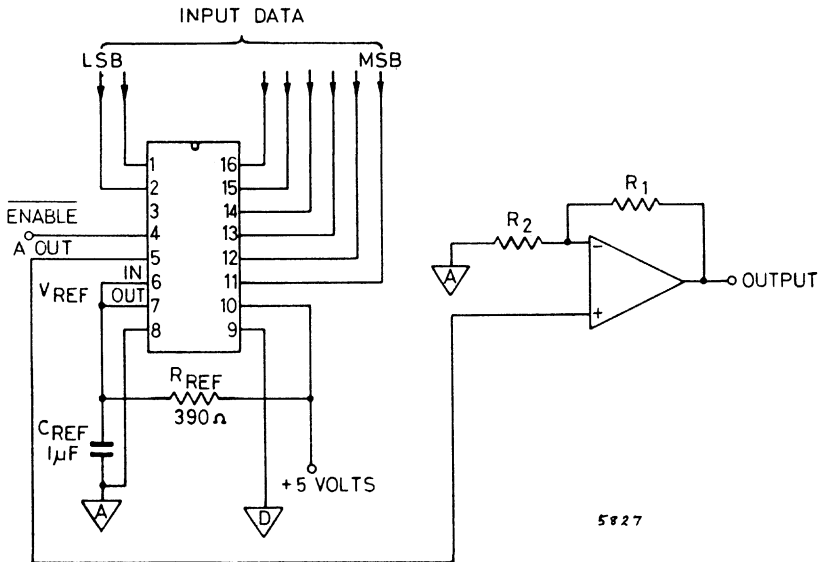
Fig. 6. Unipolar operation – Basic Circuit

66
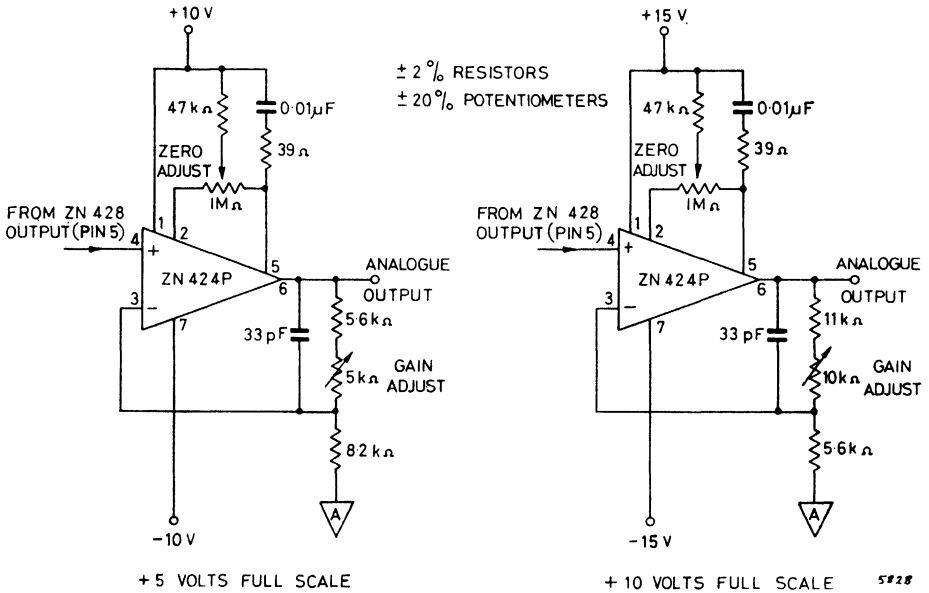
Fig. 7. Unipolar Operation – Component Values

UNIPOLAR ADJUSTMENT PROCEDURE

(i) Set all bits to OFF (low) with $\overline{\text{Enable}}$ low and adjust zero until $V_{OUT} = 0.0000$V.

(ii) Set all bits ON (high) and adjust gain until $V_{OUT} =$ FS −1 LSB.

UNIPOLAR SETTING UP POINTS

Output Range, +FS	LSB	FS − 1LSB	
+5V	19.5 mV	4.9805V	$1\text{LSB} = \dfrac{\text{FS}}{256}$
+10V	39.1 mV	9.9609V	

UNIPOLAR LOGIC CODING

Input Code (Binary)	Analogue Output (Nominal value)
11111111	FS − 1LSB
11111110	FS − 2LSB
11000000	$\frac{3}{4}$ FS
10000001	$\frac{1}{2}$ FS + 1LSB
10000000	$\frac{1}{2}$ FS
01111111	$\frac{1}{2}$ FS − 1LSB
01000000	$\frac{1}{4}$ FS
00000001	1LSB
00000000	0

(2) Bipolar D to A Converter

For bipolar operation the output from the ZN428 is offset by half full scale by connecting a resistor R_3 between $V_{REF\ IN}$ and the inverting input of the buffer amplifier (Fig. 8).
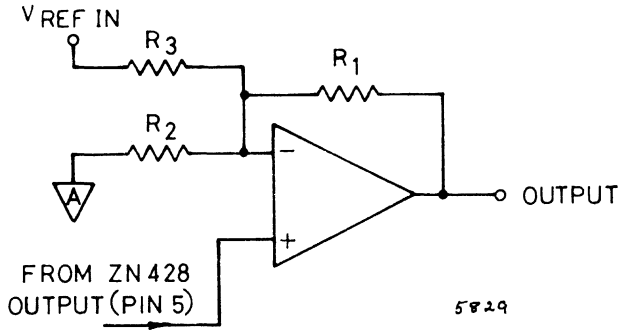
Fig. 8. Bipolar Operation – Basic Circuit

When the digital input to the ZN428 is zero the analogue output is zero and the amplifier output should be −Full scale. An input of all ones to the D to A will give a ZN428 output of $V_{REF\ IN}$ and the amplifier output required is + Full scale. Also, to match the ladder resistance the parallel combination of R_1, R_2 and R_3 should be 4 kΩ.

The nominal values of R_1, R_2 and R_3 which meet these conditions are given by

$$R_1 = 8G\ k\Omega,\ R_2 = 8G/(G\text{-}1)\ k\Omega \text{ and } R_3 = 8\ k\Omega$$

where the resultant output range is $\pm G\ V_{REF\ IN}$.

A bipolar output range of $\pm V_{REF\ IN}$ (which corresponds to the basic unipolar range 0 to $V_{REF\ IN}$) is obtained if $R_1 = R_3 = 8\ k\Omega$ and $R_2 = \infty$.

Assuming that $V_{REF\ IN} = 2.5$ volts the nominal values of resistors for $\pm 5V$ and $\pm 10V$ output ranges are given in the following table :

Output Range	G	R_1	R_2	R_3
$\pm 5V$	2	16 kΩ	16 kΩ	8 kΩ
$\pm 10V$	4	32 kΩ	10.66 kΩ	8 kΩ

Minus full scale (offset) is set by adjusting R_1 about its nominal value relative to R_3. Plus full scale (gain) is set by adjusting R_2 relative to R_1.

Practical circuit realisations are given in Fig. 9. Note that in the $\pm 5V$ case R_3 has been chosen as 7.5 kΩ (instead of 8.2 kΩ) to get a more symmetrical range of adjustment using standard potentiometers. Settling time for a major transition is 1.5 μs typical.
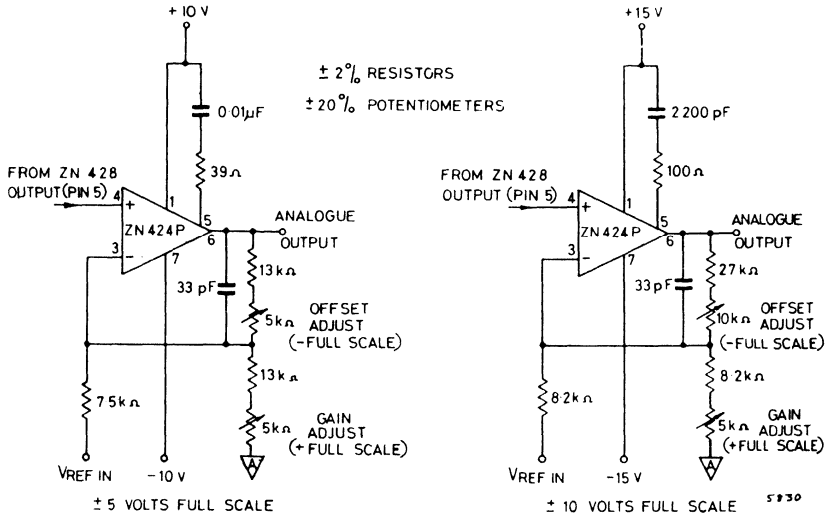
ZN428E-8/J-8

Fig. 9. Bipolar Operation – Component Values

Bipolar Adjustment Procedure

(1) Set all bits to OFF (low) with $\overline{\text{Enable}}$ low and adjust offset until the amplifier output reads −Full Scale.

(2) Set all bits ON (high) and adjust gain until the amplifier output reads + (Full Scale − 1LSB).

BIPOLAR SETTING UP POINTS

Input Range, ±FS	LSB	−FS	+(FS−1LSB)
±5V	39.1 mV	−5.0000V	+4.9609V
±10V	78.1 mV	−10.0000V	+9.9219V

$$1\text{LSB} = \frac{2\text{FS}}{256}$$

BIPOLAR LOGIC CODING

Input Code (Offset Binary)	Analogue Output (Nominal Value)
11111111	+(FS − 1LSB)
11111110	+(FS − 2LSB)
11000000	+½FS
10000001	+1LSB
10000000	0
01111111	−1LSB
01000000	−½FS
00000001	−(FS − 1LSB)
00000000	−FS

69

ZN428E-8/J-8

PIN CONNECTIONS

Bit 7 1	16 Bit 6
Bit 8 2	15 Bit 5
N.C. 3	14 Bit 4
$\overline{\text{ENABLE}}$ 4	13 Bit 3
Analogue output 5	12 Bit 2
$V_{REF\ IN}$ 6	11 Bit 1 (MSB)
$V_{REF\ OUT}$ 7	10 +V_{CC} (+5 volts)
Analogue ground 8	9 Digital ground

5131

CHIP DIMENSIONS AND LAYOUT

92 MIL

BIT 8 BIT 7 DIGITAL GND BIT 6 BIT 5

$\overline{\text{ENABLE}}$ —

— BIT 4

ANALOGUE OUTPUT —

V_{REF} IN —

— BIT 3   124 MIL

— BIT 2

V_{REF} OUT   ANALOGUE GND   +V_{CC} N.C.   BIT 1

6222

70

FERRANTI semiconductors
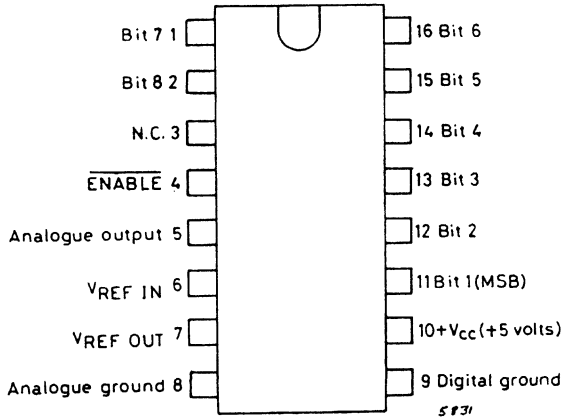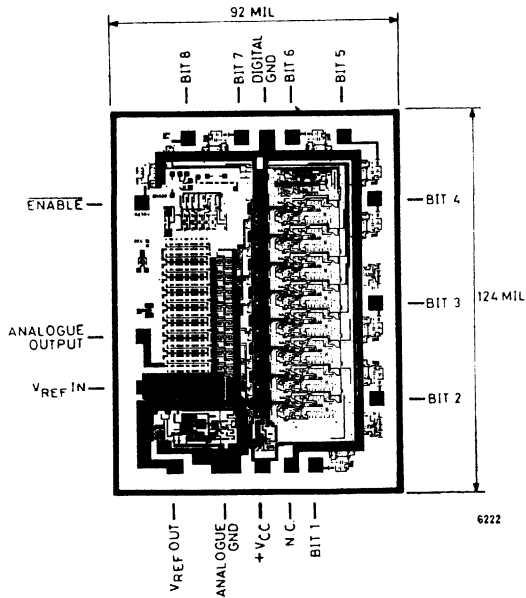
ZN429 Series

Low Cost 8 Bit Monolithic D to A Converter

FEATURES

- 8, 7 and 6-bit Accuracy
- ZN429E Series   Commercial Temp. Range   0°C to +70°C
- ZN429J-8   Military Temp. Range   −55°C to +125°C
- TTL and 5V CMOS Compatible
- Single +5V Supply
- Settling Time 1 μsec. Typical
- Designed for low-cost applications

DESCRIPTION

The ZN429 is a monolithic 8-bit digital to analogue converter containing an R-2R ladder network of diffused resistors with precision bipolar switches.

Fig. 1. System Diagram

71
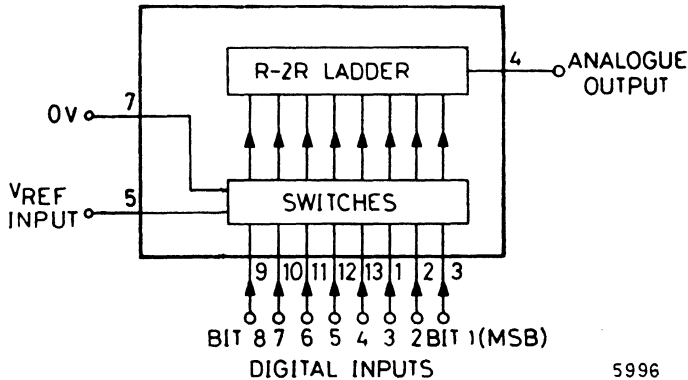
ZN429 Series

INTRODUCTION

The ZN429 is an 8-bit digital to analogue converter. It contains an advanced design of R-2R ladder network and an array of precision bipolar switches on a single monolithic chip.

The special design of ladder network results in full 8-bit accuracy using normal diffused resistors.

The converter is of the voltage switching type and uses an R-2R resistor ladder network as shown in Fig. 2.
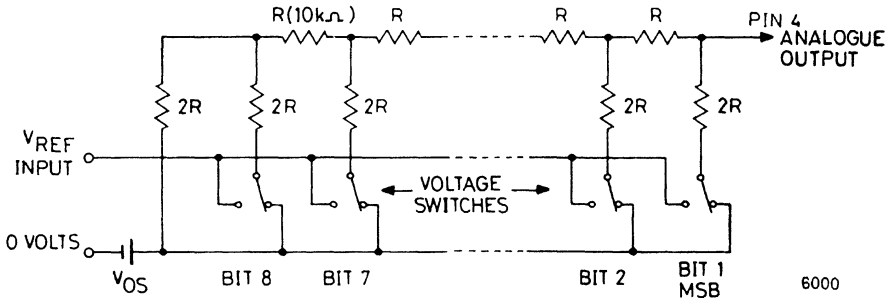
Fig. 2. The R-2R Ladder Network

Each 2R element is connected either to 0V or V_{REF} by transistor switches specially designed for low offset voltage (typically 1 millivolt).

Binary weighted voltages are produced at the output of the R-2R ladder, the value depending on the digital number applied to the bit inputs.

An external fixed or varying reference is required which should have a slope resistance less than 2 ohms.

Suggested external reference sources are the ZN404 or one of the ZN458 range. Each ZN404 is capable of supplying up to five ZN429 circuits and this is increased to ten for the ZN458 range.

ORDERING INFORMATION

Operating Temperature	8-bit accuracy	7-bit accuracy	6-bit accuracy	Package
0 to +70°C	ZN429E-8	ZN429E-7	ZN429E-6	Plastic
−55 to +125°C	ZN429J-8	—	—	Ceramic

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC} .. .. +7.0 volts

Max. voltage, logic and V_{REF} inputs .. .. +5.5 volts

Storage temperature range .. .. −55 to +125°C

CHARACTERISTICS (at $T_{amb} = 25°C$ and $V_{CC} = +5$ volts unless otherwise specified).

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Converter Resolution		8	—	—	bits	
Accuracy (useful resolution) ZN429J-8 ⎰ ZN429E-8 ⎱ ZN429E-7 ZN429E-6		8 7 6	— — —	— — —	bits bits bits	V_{REF} input = 2.0 to 3.0 volts
Non-linearity		—	—	±0.5	L.S.B.	*Note 1*
Differential non-linearity		—	±0.5	—	L.S.B.	*Note 2*
Settling time to 0.5 L.S.B.		—	1.0	—	µs	1 L.S.B. step
Settling time to 0.5 L.S.B.		—	2.0	—	µs	All bits ON to OFF or OFF to ON
Offset voltage ZN429J-8 ZN429E-8 ⎱ ZN429E-7 ⎬ ZN429E-6 ⎰	V_{OS}	— —	5.0 3.0	8.0 5.0	mV mV	All bits OFF *Note 1*
V_{OS} temperature coefficient		—	5	—	µV/°C	
Full scale output		2.545	2.550	2.555	volts	All bits ON Ext. V_{REF} = 2.560V
Full scale temp. coefficient		—	3	—	ppm/°C	Ext. V_{REF} = 2.560V
Non-linearity temp. coeff.		—	7.5	—	ppm/°C	Relative to F.S.R.

Notes:

1. The ZN429J-8 differs from the ZN429E-8 in the following respects:
   (a) For the ZN429J-8, the maximum linearity error may increase to ±0.4% FSR i.e. ±1 LSB over the temperature ranges −55°C to 0°C and +70°C to +125°C.
   (b) Offset voltage. The difference is due to package lead resistance. This offset will normally be removed by the setting up procedure, and because the offset temperature coefficient is low, the specified accuracy will be maintained.

2. Monotonic over full temperature range at resolution appropriate to accuracy.

ZN429 Series

CHARACTERISTICS (*continued*)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Analogue output resistance	R_o	—	10	—	kΩ	
External reference voltage		0	—	3.0	volts	
Supply voltage	V_{CC}	4.5	—	5.5	volts	
Supply current	I_s	—	5	9	mA	
High level input voltage	V_{IH}	2.0	—	—	volts	
Low level input voltage	V_{IL}	—	—	0.7	volts	
High level input current	I_{IH}	—	—	10	μA	V_{CC} = max., V_I = 2.4V
		—	—	100	μA	V_{CC} = max., V_I = 5.5V
Low level input current	I_{IL}	—	—	−0.18	mA	V_{CC} = max., V_I = 0.3V

APPLICATIONS

1. 8-bit D to A Converter

The ZN429 gives an analogue voltage output directly from pin 4 therefore the usual current to voltage converting amplifier is not required. The output voltage drift, due to the temperature coefficient of the Analogue Output Resistance R_o, will be less than 0.004% per °C (or 1 L.S.B./100°C) if R_L is chosen to be ⩾650 kΩ

In order to remove the offset voltage and to calibrate the converter a buffer amplifier is necessary. Fig. 3 shows a typical scheme using the internal reference voltage. To minimise temperature drift in this and similar applications the source resistance to the inverting input of the operational amplifier should be approximately 6 kΩ. The calibration procedure is as follows:

i. Set all bits to OFF (low) and adjust R_2 until V_{out} = 0.000V.

ii. Set all bits to ON (high) and adjust R_1 until V_{out} = Nominal full scale reading −1 L.S.B.

iii. Repeat *i.* and *ii.*

$$\text{e.g. Set F.S.R. to } +3.840 \text{ volts} - 1 \text{ L.S.B.}$$
$$= 3.825 \text{ volts}$$

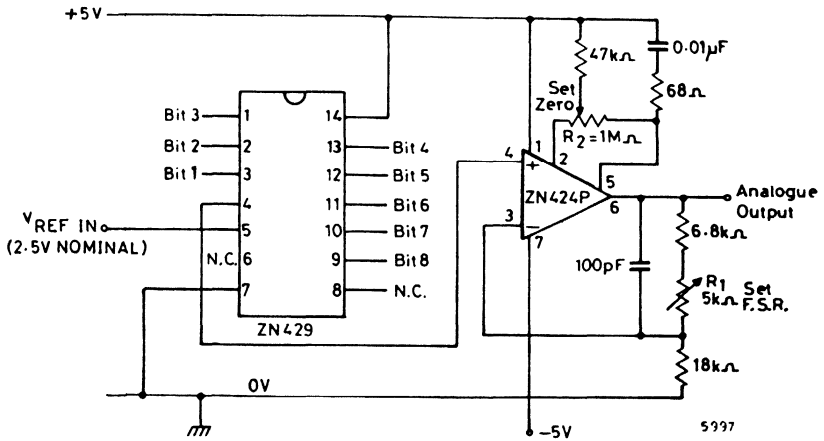$$(1 \text{ L.S.B.} = \frac{3.84}{256} = 15.0 \text{ millivolts})$$

74

Fig. 3. 8-bit Digital to Analogue Converter

Alternative Output Buffer using the ZLD741

The following circuit, employing the ZLD741 operational amplifier, may be used as the output buffer (Fig. 3).
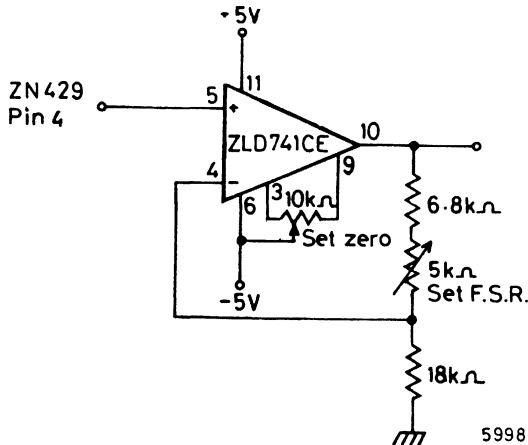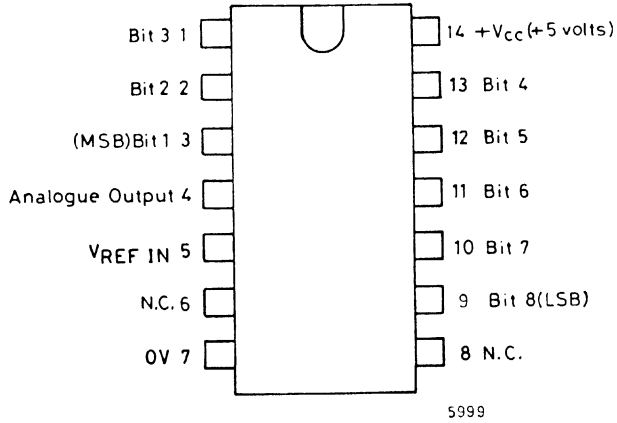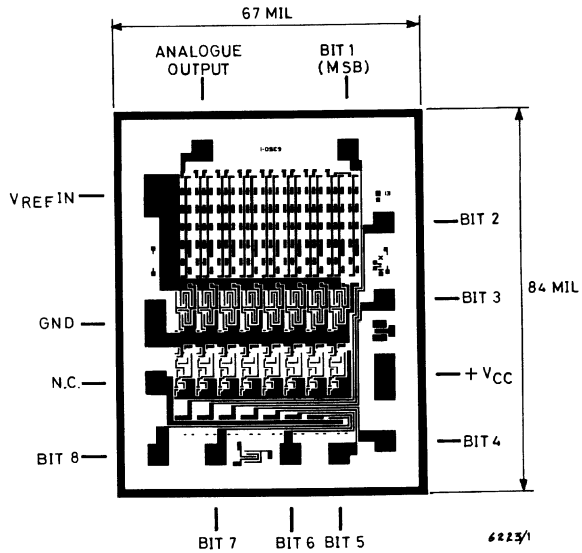

Fig. 4. The ZLD741 as Output Buffer

75

ZN429 Series

PIN CONNECTIONS

Bit 3	1	14 +V$_{CC}$ (+5 volts)
Bit 2	2	13 Bit 4
(MSB)Bit 1	3	12 Bit 5
Analogue Output	4	11 Bit 6
V$_{REF}$ IN	5	10 Bit 7
N.C.	6	9 Bit 8(LSB)
OV	7	8 N.C.

5999

CHIP DIMENSIONS AND LAYOUT

67 MIL

ANALOGUE OUTPUT   BIT 1 (MSB)

V$_{REF}$ IN

GND

N.C.

BIT 8

BIT 2

BIT 3

+ V$_{CC}$

BIT 4

84 MIL

BIT 7   BIT 6   BIT 5

6223/1

FERRANTI semiconductors

10-Bit Successive Approximation Monolithic A/D Converter

FEATURES

- 10, 9 and 8-Bit Accuracies
- 3 Operating Temperature Ranges
- 20 µs Conversion Time Guaranteed
- Input Range as Desired
- ±5V Supplies, TTL/CMOS Compatible
- Parallel and Serial Outputs
- Bipolar Monolithic Construction

DESCRIPTION

The ZN432 range of successive approximation analogue to digital converters combine several innovations to provide this function on a fully monolithic silicon integrated circuit. The chip contains a current switching array using a matrix of diffused resistors (no trim required), successive approximation logic with TTL interfacing, 2.5V precision voltage reference with reference amplifier, and fast comparator with good overload recovery. The overall accuracy of the A-D system is sufficient to provide guaranteed monotonicity over the operating temperature range.
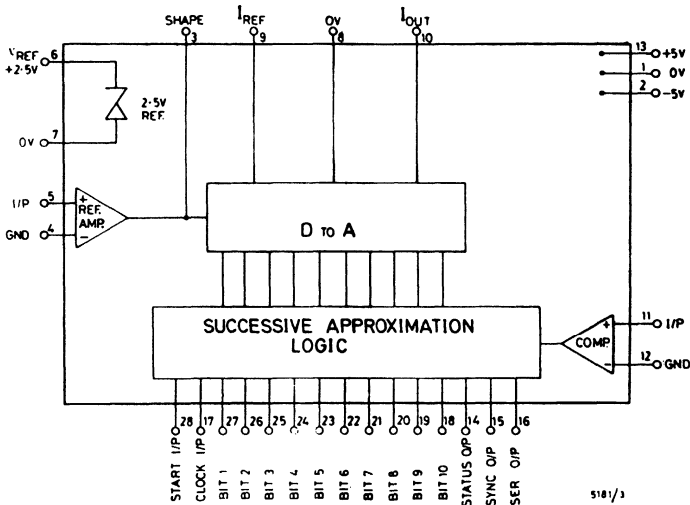
Fig. 1 – INTEGRATED CIRCUIT BLOCK DIAGRAM

77

ZN432 Series
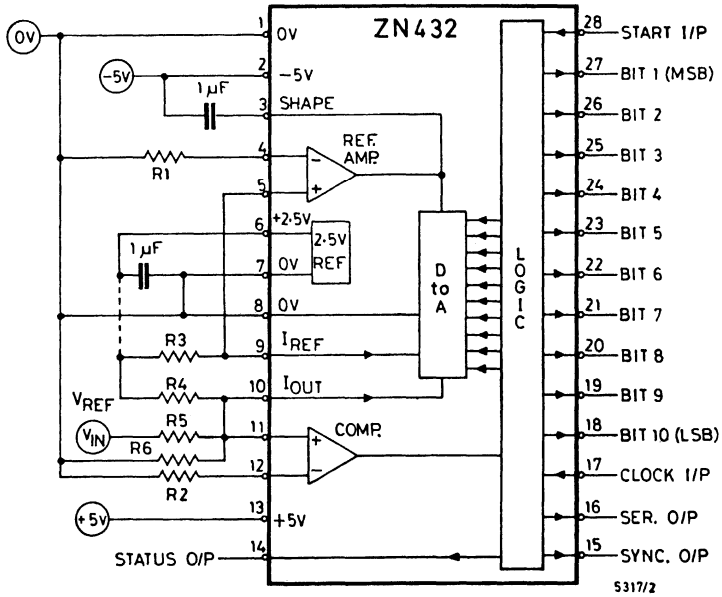
Fig. 2 – TYPICAL EXTERNAL COMPONENTS

ORDERING INFORMATION

Operating Temperature	10-bit accuracy	9-bit accuracy	8-bit accuracy	Package
−55 to +125°C	ZN432J-10	ZN432J-9	ZN432J-8	Ceramic
−40 to +85°C	ZN432BJ-10	ZN432BJ-9	ZN432BJ-8	Ceramic
0 to +70°C	ZN432CJ-10	ZN432CJ-9	ZN432CJ-8	Ceramic

ABSOLUTE MAXIMUM RATINGS

Supply Voltages .. .. ± 7 volts
Logic Input Voltage .. .. .. $+V_{CC}$ and 0V
Storage Temperature Range .. $-55°C$ to $+125°C$

CHARACTERISTICS (at $\pm 5V$ supplies and internal reference unless otherwise specified).

Parameter	Version	$t_{amb} = +25°C$			Over Spec. Temp. Range		Units	Conds.
		Min.	Typ.	Max.	Min.	Max.		
CONVERTER Accuracy (useful resolution)	ZN432J-10 ZN432BJ-10 ZN432CJ-10	10			10		Bits	Note 1
	ZN432J-9 ZN432BJ-9 ZN432CJ-9	9			9		Bits	
	ZN432J-8 ZN432BJ-8 ZN432CJ-8	8			8		Bits	
Non-linearity	All types			± 0.5			LSB	
Differential non-linearity	All types		± 0.5				LSB	Note 1
Operating temp. range	ZN432J-10 ZN432J-9 ZN432J-8				-55	$+125$	°C	
	ZN432BJ-10 ZN432BJ-9 ZN432BJ-8				-40	$+85$	°C	
	ZN432CJ-10 ZN432CJ-9 ZN432CJ-8				0	$+70$	°C	
D to A reference current, I_{REF} (pin 9)	All types	0.25		1.0	0.25	1.0	mA	Note 6
Conversion time	All types		15	20		20	μs	Note 2
Nominal analogue input range	All types	-2.5		$+2.5$			V	Note 3
Supply rejection	All types		0.1				% per V	
Gain error	All types		± 0.05				%	Note 4

79

ZN432 Series

CHARACTERISTICS (*continued*)

Parameter	Version	$t_{amb} = +25°C$			Over Spec. Temp. Range		Units	Conds.
		Min.	Typ.	Max.	Min.	Max.		
Gain temperature coefficient (Note 4)	ZN432J-10 ZN432BJ-10 ZN432CJ-10		10				ppm/°C	
	ZN432J-9 ZN432BJ-9 ZN432CJ-9 ZN432J-8 ZN432BJ-8 ZN432CJ-8		20				ppm/°C	
Zero temperature coefficient	ZN432J-10 ZN432BJ-10 ZN432CJ-10		7				ppm/°C of FSR	
	ZN432J-9 ZN432BJ-9 ZN432CJ-9 ZN432J-8 ZN432BJ-8 ZN432CJ-8		15				ppm/°C of FSR	
Supply voltage	All types	±4.5	±5	±5.5	±4.5	±5.5	V	
Supply current	All types		35				mA	
Power consumption	All types		350				mW	
INTERNAL VOLTAGE REFERENCE Output voltage	All types		2.480				V	
Output voltage tolerance (Note 5)	ZN432J-10 ZN432BJ-10 ZN432CJ-10			±1.5			%	
	ZN432J-9 ZN432BJ-9 ZN432CJ-9			±2.0			%	
	ZN432J-8 ZN432BJ-8 ZN432CJ-8			±5.0			%	
Slope impedance	All types		0.75				Ω	
Maximum Reference load current			±2				mA	

CHARACTERISTICS *(continued)*

Parameter	Version	$t_{amb} = +25°C$			Over Spec. Temp. Range		Units	Conditions
		Min.	Typ.	Max.	Min.	Max.		
LOGIC	All types							
High level input voltage		2.0			2.0		V	
Low level input voltage				0.8		0.8	V	
High level input current			7				μA	$V_S = \pm5.5V$ $V_I = 2.4V$
			50				μA	$V_S = \pm5.5V$ $V_I = 5.5V$
Low level input current			1				μA	$V_S = \pm5.5V$ $V_I = 0.4V$
High level output voltage		2.4			2.4		V	$I_{load} = -40\,μA$
Low level output voltage				0.4		0.4	V	$I_{load} = 1.6\,mA$

NOTE 1. No missing codes over full temperature range at resolution appropriate to accuracy.

NOTE 2. This corresponds to a maximum clock rate of 550 kHz based on 11 clock periods per conversion cycle (see timing diagram, page 84). This provides an update rate of 45 kHz.

NOTE 3. Single polarity and other input ranges may be provided by different input resistor values. (see page 7)

NOTE 4. Excluding reference.

NOTE 5. For typical temperature performance see Fig. 6, page 85.

NOTE 6. The full scale D to A output current $I_{OUT} = 4$ times I_{REF}. For optimum performance $I_{REF} = 0.5$ mA.

ZN432 Series
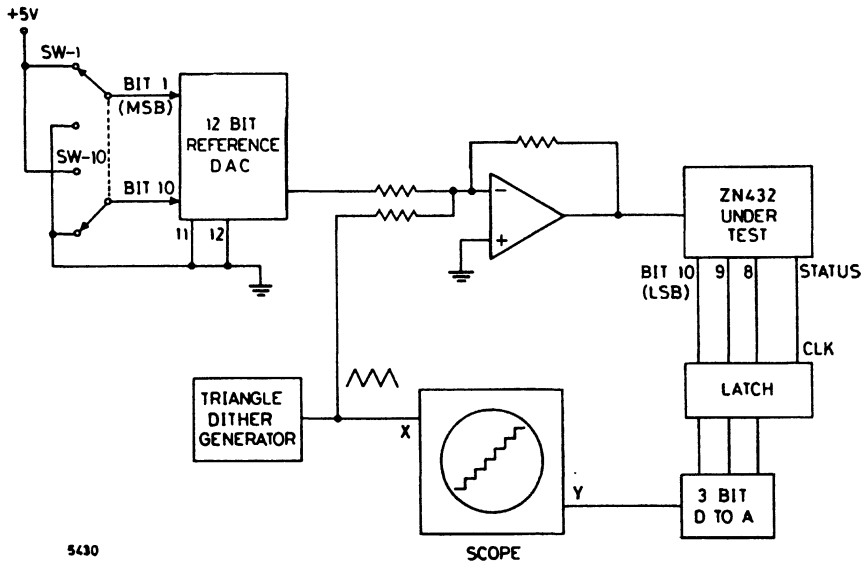
Fig. 3 – DYNAMIC CROSSPLOT ACCURACY TEST

Switches SW-1 to SW-10 are set to the appropriate digital code to select the point on the character-istic to be displayed. For example, code 10000 00000 would select half full scale, i.e. the major transition.

The output from the dither generator (suggested peak to peak amplitude $= \pm 4 \times$ L.S.B.) is used as the X deflection for the scope and is also superimposed on the analogue output from the reference D.A.C. in the summing amplifier. The resulting analogue signal including dither is used as V_{IN} for the ZN432 under test.

Bit 10, 9 and 8 outputs are fed to the inputs of a 3-bit D.A.C. of at least 6-bit accuracy and the analogue output used as the Y deflection for the scope. Differential non-linearity is shown by horizontal lines which are longer or shorter than the rest.

CALCULATION OF EXTERNAL RESISTORS (See Fig. 2, page 78).

1. R_3, R_4, R_5 can affect gain and offset stability and thus require to be of high quality.

2. R_1 and R_2 are to allow for the bias current of the reference amplifier and comparator, thus:
$$R_1 = R_3$$
And R_2 = parallel combination of R_4, R_5 and R_6.

3. I_{REF} should be 0.5 mA

   Therefore
$$R_3 = \frac{V_{REF}}{0.5 \text{ mA}}$$

   $I_{out\ FS}$ is four times I_{REF}, i.e., 2 mA

4. Analysing the network yields the following:
$$R_4 = \frac{-V_{REF}\ R_5}{V_{in}\ min}$$
$$R_5 = \frac{V_{in}\ max - V_{in}\ min}{I_{out\ FS}}$$

   Where V_{in} max is the voltage for the logic output to be all 1's.
   V_{in} min is the voltage for the logic output to be all 0's.

5. R_6 should be chosen such that the parallel combination of R_4, R_5 and R_6 is about 1.25 kΩ as this determines the D to A time constant and hence conversion time.

6. The following is a table of values to give examples of the above equations.

V_{in} max	V_{in} min	V_{REF}	R_1[1]	R_2[1]	R_3	R_4	R_5	R_6[1]
+2.5	−2.5	2.5	5 kΩ	1.25 kΩ	5 kΩ	2.5 kΩ	2.5 kΩ	∞
+2.5	−2.5	5 *	10 kΩ	1.25 kΩ	10 kΩ	5 kΩ	2.5 kΩ	5 kΩ
+2.5	0	2.5	5 kΩ	1.25 kΩ	5 kΩ	∞	1.25 kΩ	∞
+5	0	2.5	5 kΩ	1.25 kΩ	5 kΩ	∞	2.5 kΩ	2.5 kΩ
+4	−2	2.5	5 kΩ	1.25 kΩ	5 kΩ	3.75 kΩ	3 kΩ	5 kΩ
+4	−2	12 *	24 kΩ	1.25 kΩ	24 kΩ	3.75 kΩ	3 kΩ	5 kΩ
+10	−10	2.5	5 kΩ	1.25 kΩ	5 kΩ	2.5 kΩ	10 kΩ	3.33 kΩ

Note 1. Nearest preferred value may be used for R_1, R_2 and R_6
*Note 2. External reference

7. For setting up R_4 will adjust the offset.
   R_3 will adjust the gain.
For unipolar operation where R_4 approaches ∞ and a zero adjustment is required, the following offset circuit is suggested in place of R_4 (Typical values only).

PINS 10 11 ───/\/\/─── ───/\/\/─── PIN 12
100 kΩ   1 MΩ   100 kΩ
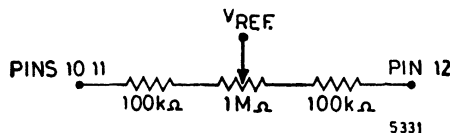   5331

Fig. 4 – OFFSET CIRCUIT WITH UNIPOLAR OPERATION
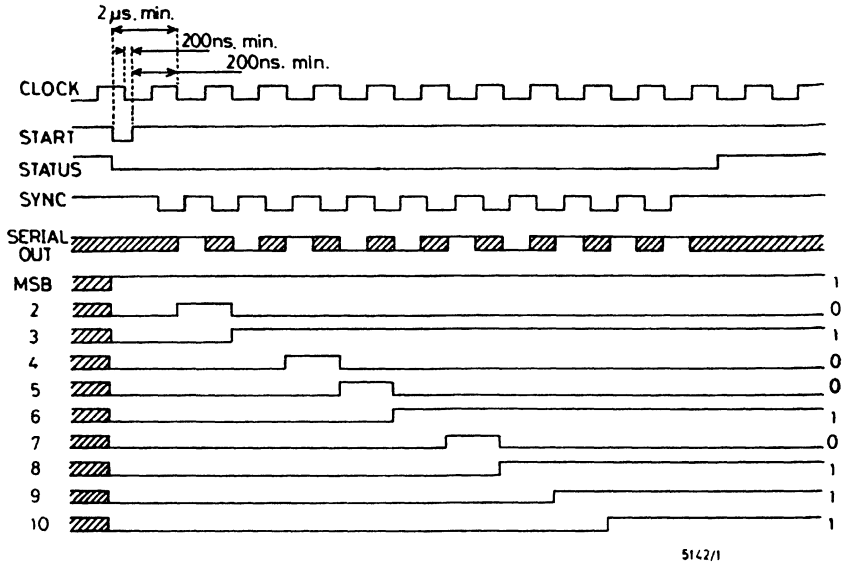
ZN432 Series

TIMING DETAILS

Fig. 5 – TIMING DIAGRAM

NOTES ON TIMING DIAGRAM

1. Conversion is initiated by a 'START' pulse which sets the MSB to 1 and all the other bits to 0.

2. The first active (negative going) edge of Clock after the trailing edge of the 'START' pulse should not occur until at least 2 μs after the leading edge of the 'START' pulse to allow for MSB settling.

3. A negative going edge of Clock must not occur within 200 ns either side of the trailing edge of the 'START' pulse.

4. As a special case of conditions (2) and (3) the 'START' pulse may be coincident with, and of the same duration as, a negative going clock pulse.

5. Serial data is available during conversion at the Serial Output.
   Ten SYNC pulses are provided to facilitate data transmission.
   The serial output data is valid on the positive going edge of the SYNC pulse.

6. Cross hatching indicates a 'don't care' condition or, in the case of serial output, invalid data.

7. The conversion sequence shown is for the digital word 1010010111.

8. The parallel output data is valid when the Status Output goes HIGH.

84

LOGIC CODING

Table 1. Unipolar Operation

Analogue Input Notes 1, 2	Digital Output Code MSB LSB
FS −1LSB	1111111111
FS −2LSB	1111111110
$\frac{3}{4}$ FS	1100000000
$\frac{1}{2}$ FS +1LSB	1000000001
$\frac{1}{2}$ FS	1000000000
$\frac{1}{2}$ FS −1LSB	0111111111
$\frac{1}{4}$ FS	0100000000
1LSB	0000000001
0	0000000000

Table 2. Bipolar Operation

Analogue Input Notes 1, 2	Digital Output Code MSB LSB
+(FS −1LSB)	1111111111
+(FS −2LSB)	1111111110
+($\frac{1}{2}$ FS)	1100000000
+(1LSB)	1000000001
0	1000000000
−(1LSB)	0111111111
−($\frac{1}{2}$ FS)	0100000000
−(FS−1LSB)	0000000001
−FS	0000000000

NOTES:

1. Analogue inputs shown are nominal centre values of code.

2. "FS" is full scale.

OFFSET AND GAIN SETTING

For unipolar, supply an input of $\frac{1}{2}$ LSB for transition 0000000000 to 0000000001, and of (full scale −1$\frac{1}{2}$ LSB) for transition 1111111111 to 1111111110.

For bipolar, supply an input of −(full scale −$\frac{1}{2}$ LSB) for transition 0000000000 to 0000000001, and of (full scale −1$\frac{1}{2}$ LSB) for transition 1111111111 to 1111111110.
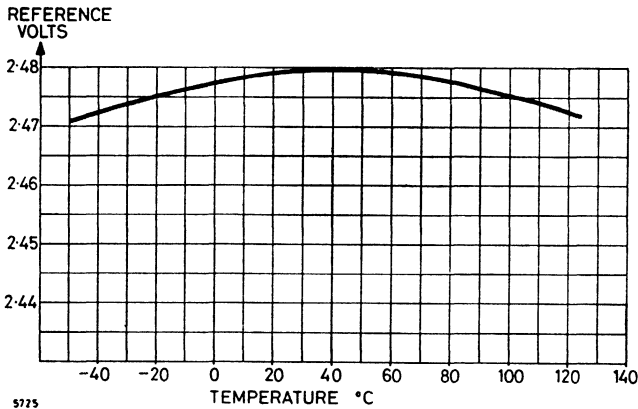
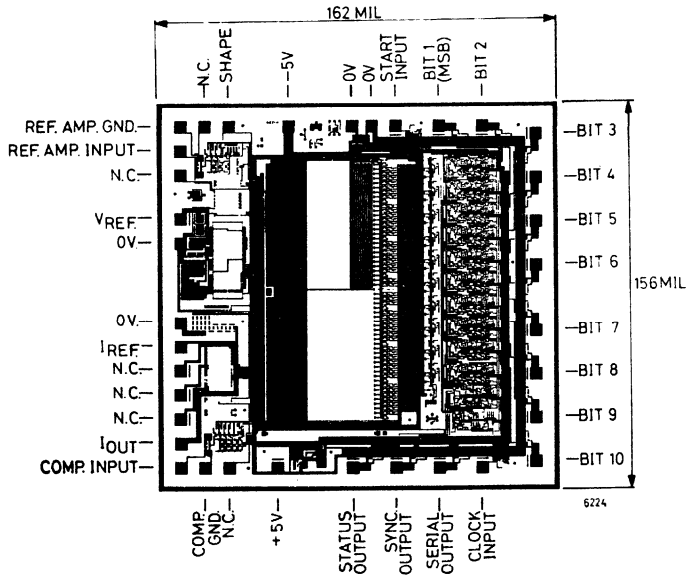Fig. 6 – TYPICAL REFERENCE VOLTAGE v TEMPERATURE (ALL TYPES)

ZN432 Series

PIN CONNECTIONS

Left	Pin		Pin	Right
0V	1		28	START I/P
−5V	2		27	BIT 1 (MSB)
SHAPE	3		26	BIT 2
REF. AMP. GND.	4		25	BIT 3
REF. AMP. I/P	5		24	BIT 4
$V_{REF.}$ +2·48V	6		23	BIT 5
0V	7		22	BIT 6
0V	8		21	BIT 7
I REF	9		20	BIT 8
I OUT	10		19	BIT 9
COMP. I/P	11		18	BIT 10 (LSB)
COMP. GND.	12		17	CLOCK I/P
+5V	13		16	SERIAL O/P
STATUS O/P	14		15	SYNC O/P

5140/2

CHIP DIMENSIONS AND LAYOUT

6224

86

FERRANTI semiconductors
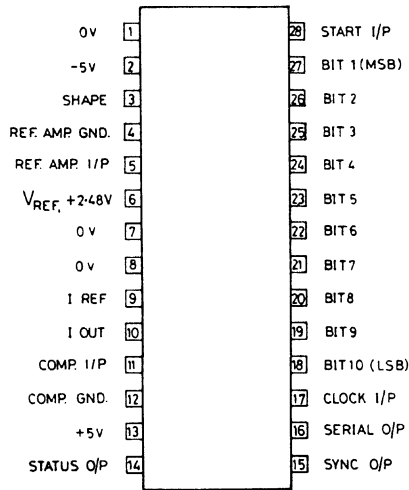
10-Bit Tracking Monolithic A/D Converter

FEATURES

● **10, 9 and 8-Bit Accuracies**
● **3 Operating Temperature Ranges**
● **1µs Conversion Time (Assuming Continuous Tracking)**
● **Input Range as Desired**
● **±5V Supplies, TTL/CMOS Compatible**
● **Parallel and Serial Outputs**
● **Bipolar Monolithic Construction**

DESCRIPTION

The ZN433 range of tracking analogue to digital converters combines several innovations to provide this function on a fully monolithic silicon integrated circuit. The chip contains a current switching array using a matrix of diffused resistors (no trim required), tracking logic with TTL interfacing, 2.5V precision voltage reference with reference amplifier, and fast window comparator with good overload recovery. At a resolution appropriate to the accuracy specification, no missing codes are obtained over the full temperature range.

The tracking principle ensures continuous up to date conversion data. This is suitable for single channel conversion, e.g. digital transducers, and often obviates the need for sample and hold.
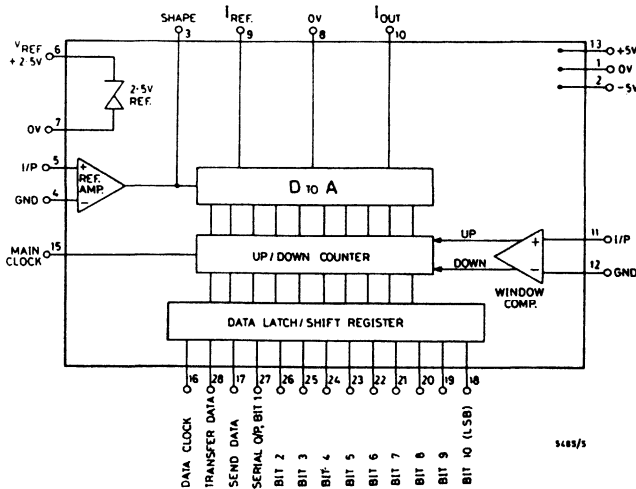
Fig. 1 – SYSTEM DIAGRAM

ZN433 Series
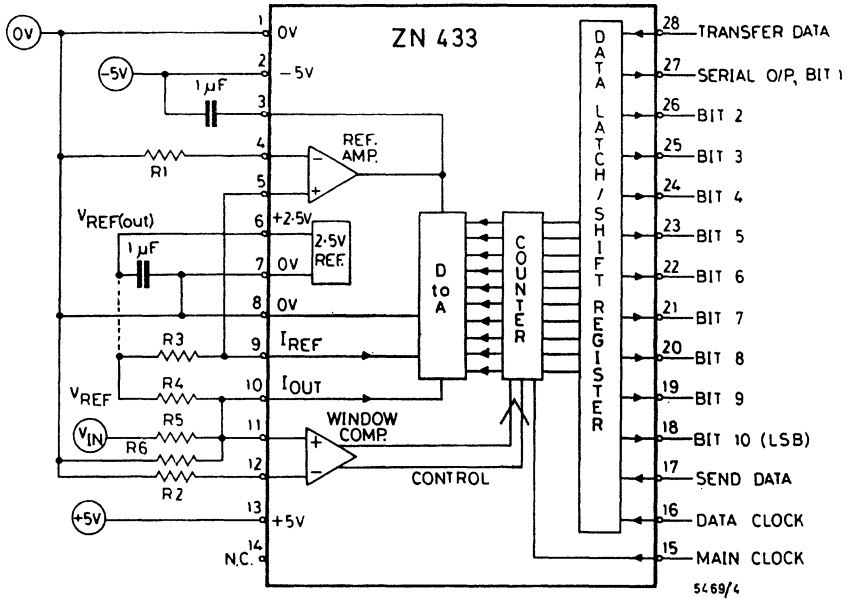
Fig. 2 – TYPICAL EXTERNAL COMPONENTS

See page 93 for calculation of resistor values. When the internal reference is used, $V_{REF(out)}$ (pin 6) is connected to R3 and R4 as shown. An external reference may also be used, which for ratiometric operation can vary by $\pm20\%$ of nominal.

ORDERING INFORMATION

Operating Temperature	10-bit accuracy	9-bit accuracy	8-bit accuracy	Package
−55 to +125°C	ZN433J-10	ZN433J-9	ZN433J-8	Ceramic
−40 to +85°C	ZN433BJ-10	ZN433BJ-9	ZN433BJ-8	Ceramic
0 to +70°C	ZN433CJ-10	ZN433CJ-9	ZN433CJ-8	Ceramic

ABSOLUTE MAXIMUM RATINGS

Supply Voltages .. .. ±7 volts
Logic Input Voltage .. .. .. +V_{CC} and 0V
Storage Temperature Range .. .. −55°C to +125°C

CHARACTERISTICS (at ±5V supplies and internal reference unless otherwise specified).

Parameter	Version	$T_{amb} = +25°C$			Over Spec. Temp. Range		Units	Conds.
		Min.	Typ.	Max.	Min.	Max.		
CONVERTER								
Accuracy (useful resolution)	ZN433J-10 ZN433BJ-10 ZN433CJ-10	10			10		Bits	Note 1
	ZN433J-9 ZN433BJ-9 ZN433CJ-9	9			9		Bits	
	ZN433J-8 ZN433BJ-8 ZN433CJ-8	8			8		Bits	
Non-linearity	All types			±0.5			LSB	
Differential non-linearity	All types		±0.5				LSB	Note 1
Operating temp. range	ZN433J-10 ZN433J-9 ZN433J-8				−55	+125	°C	
	ZN433BJ-10 ZN433BJ-9 ZN433BJ-8				−40	+85	°C	
	ZN433CJ-10 ZN433CJ-9 ZN433CJ-8				0	+70	°C	
D to A reference current, I_{REF} (pin 9)	All types	0.8		1.2	0.8	1.2	mA	Note 2
Max. Clock Rate	All types	1	1.2		1		MHz	Note 3
Nominal analogue input range	All types	−2.5		+2.5			V	Note 4
Supply rejection	All types		0.1				% per V	

ZN433 Series

CHARACTERISTICS *(continued)*

Parameter	Version	$T_{amb} = +25°C$			Over Spec. Temp. Range		Units	Conds.
		Min.	Typ.	Max.	Min.	Max.		
Gain temperature coefficient (Note 5)	ZN433J-10 ZN433BJ-10 ZN433CJ-10		10				ppm/°C	
	ZN433J-9 ZN433BJ-9 ZN433CJ-9 ZN433J-8 ZN433BJ-8 ZN433CJ-8		20				ppm/°C	
Zero temperature coefficient	ZN433J-10 ZN433BJ-10 ZN433CJ-10		7				ppm/°C of FSR	
	ZN433J-9 ZN433BJ-9 ZN433CJ-9 ZN433J-8 ZN433BJ-8 ZN433CJ-8		15				ppm/°C of FSR	
Supply voltage	All types	±4.5	±5	±5.5	±4.5	±5.5	V	
Supply current	All types		50				mA	
Power consumption	All types		500				mW	
INTERNAL VOLTAGE REFERENCE Output voltage	All types		2.480				V	
Output voltage tolerance (Note 6	ZN433J-10 ZN433BJ-10 ZN433CJ-10			±1.5			%	
	ZN433J-9 ZN433BJ-9 ZN433CJ-9			±2.0			%	
	ZN433J-8 ZN433BJ-8 ZN433CJ-8			±5.0			%	
Slope impedance	All types		0.75				Ω	
Maximum reference load current			±4				mA	

90

CHARACTERISTICS *(continued)*

Parameter	Version	$T_{amb} = +25°C$			Over Spec. Temp. Range		Units	Conditions
		Min.	Typ.	Max.	Min.	Max.		
LOGIC	All types							
High level input voltage		2.0			2.0		V	
Low level input voltage				0.8		0.8	V	
High level input current			7				μA	$V_S = ±5.5V$ $V_I = 2.4V$
			50				μA	$V_S = ±5.5V$ $V_I = 5.5V$
Low level input current			1				μA	$V_S = ±5.5V$ $V_I = 0.4V$
High level output voltage		2.4			2.4		V	$I_{load} = -40 μA$
Low level output voltage				0.4		0.4	V	$I_{load} = 1.6 mA$

NOTE 1. No missing codes over full temperature range at resolution appropriate to accuracy.

NOTE 2. The full scale D to A output current $I_{out} = 4$ times I_{REF}. For optimum performance $I_{REF} = 1.0$ mA.

NOTE 3. For main clock waveform see Fig. 5, page 94. Input signals which do not change by more than 1 LSB/μs may be tracked continuously without the need for a sample and hold. This corresponds to a full scale bandwidth of 300 Hz. Higher frequencies may be tracked if the amplitude is reduced, e.g. the half full scale bandwidth is 600 Hz.

NOTE 4. Single polarity and other input ranges may be provided by different input resistor values (see page 93).

NOTE 5. Excluding reference.

NOTE 6. For typical temperature performance see Fig. 6, page 95.

ZN433 Series
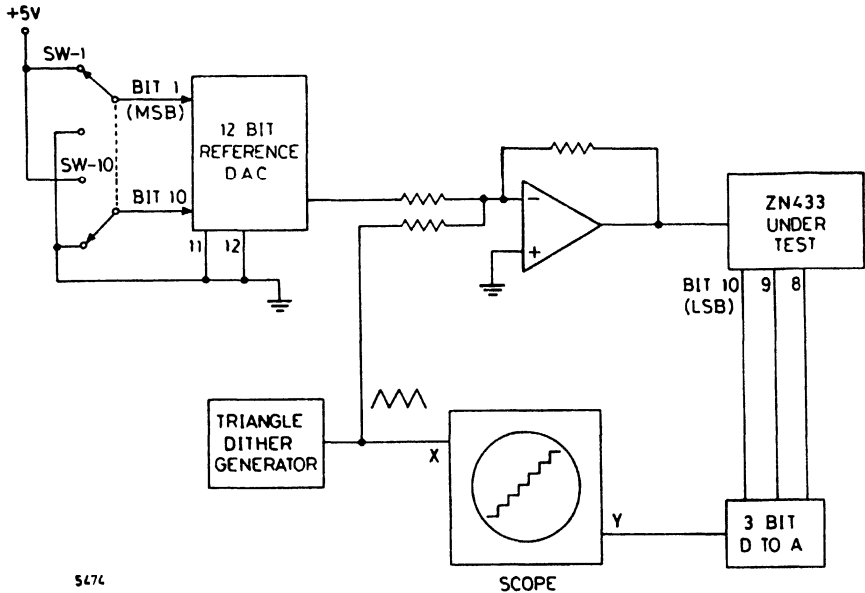
Fig. 3 – DYNAMIC CROSSPLOT ACCURACY TEST

Switches SW-1 to SW-10 are set to the appropriate digital code to select the point on the characteristic to be displayed. For example, code 10000 00000 would select half full scale, i.e. the major transition.

The output from the dither generator (suggested peak to peak amplitude = $\pm 4 \times$ L.S.B.) is used as the X deflection for the scope and is also superimposed on the analogue output from the reference D.A.C. in the summing amplifier. The resulting analogue signal including dither is used as V_{IN} for the ZN433 under test.

Bit 10, 9 and 8 outputs are fed to the inputs of a 3 bit D.A.C. of at least 6 bit accuracy and the analogue output used as the Y deflection for the scope. Differential non-linearity is shown by horizontal lines which are longer or shorter than the rest.

CALCULATION OF EXTERNAL RESISTORS (See Fig. 2, page 88).

1. R_3, R_4, R_5 can affect gain and offset stability and thus require to be of high quality.
2. R_1 and R_2 are to allow for the bias current of the reference amplifier and comparator which both operate in a virtual earth mode. Thus: $R_1 = R_3$
   And R_2 = parallel combination of R_4, R_5 and R_6.
3. I_{REF} should be 1.0 mA, though it may be varied from 0.8 mA to 1.2 mA,

   Therefore
   $$R_3 = \frac{V_{REF}}{1.0 \text{ mA}}$$

   $I_{out\ FS}$ is four times I_{REF}, i.e., 4 mA (I_{out} for zero reading is 0 mA).
4. Analysing the network yields the following:
   $$R_4 = \frac{-V_{REF}\ R_5}{V_{in}\ min}$$
   $$R_5 = \frac{V_{in}\ max - V_{in}\ min}{I_{out\ FS}}$$
   Where V_{in} max is the voltage for the logic output to be all 1's.
   V_{in} min is the voltage for the logic output to be all 0's.
5. R_6 should be chosen such that the parallel combination of R_4, R_5 and R_6 is about 625Ω as this determines the D to A time constant and hence conversion time.
6. The following is a table of values to give examples of the above equations.

V_{in} max	V_{in} min	V_{REF}	R_1[1]	R_2[1]	R_3	R_4	R_5	R_6[1]
+2.5	−2.5	2.5	2.5 kΩ	625Ω	2.5 kΩ	1.25 kΩ	1.25 kΩ	∞
+2.5	−2.5	5[*]	5 kΩ	625Ω	5 kΩ	2.5 kΩ	1.25 kΩ	2.5 kΩ
+2.5	0	2.5	2.5 kΩ	625Ω	2.5 kΩ	∞	625Ω	∞
+5	0	2.5	2.5 kΩ	625Ω	2.5 kΩ	∞	1.25 kΩ	1.25 kΩ
+4	−2	2.5	2.5 kΩ	625Ω	2.5 kΩ	1.875 kΩ	1.5 kΩ	2.5 kΩ
+4	−2	12[*]	12 kΩ	625Ω	12 kΩ	1.875 kΩ	1.5 kΩ	2.5 kΩ
+10	−10	2.5	2.5 kΩ	625Ω	2.5 kΩ	1.25 kΩ	5 kΩ	1.67 kΩ

Note 1. Nearest preferred value may be used for R_1, R_2 and R_6
*Note 2. External reference

7. For setting up: R_4 will adjust the offset.
   R_3 will adjust the gain.
For unipolar operation where R_4 approaches ∞ and a zero adjustment is required, the following offset circuit is suggested in place of R_4 (Typical values only).
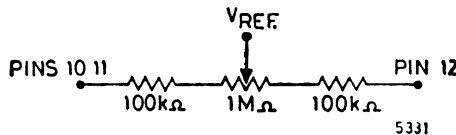

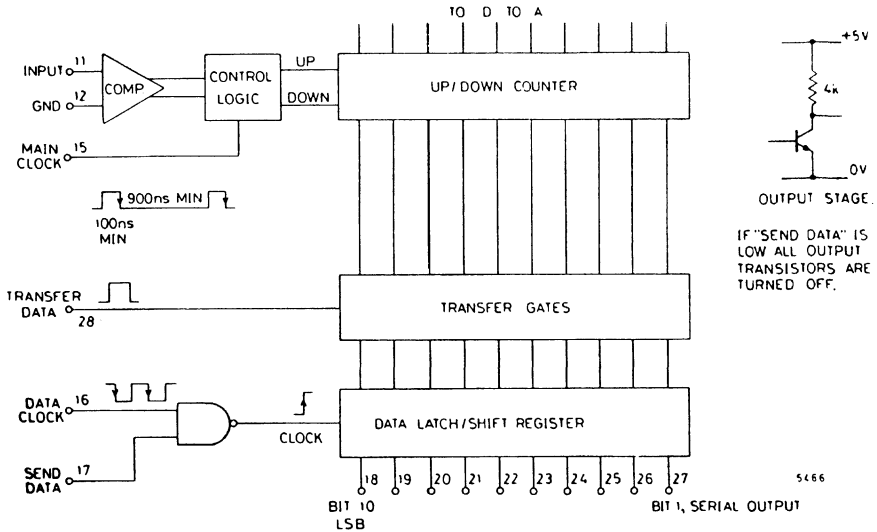Fig. 4 – OFFSET CIRCUIT WITH UNIPOLAR OPERATION

ZN433 Series

LOGIC DETAILS

Fig. 5 – LOGIC SYSTEM

NOTES ON LOGIC DIAGRAM

1. The Window Comparator and Control Logic determine whether the Counter will clock up or down or keep the same value on an active (negative going) edge of the Main Clock.

2. Parallel data from the Up/Down Counter will be loaded into the output Data Latch/Shift Register when the TRANSFER DATA input is HIGH. TRANSFER DATA should not be taken HIGH until 150 ns after the MAIN CLOCK edge and should go LOW before the next MAIN CLOCK edge. The minimum TRANSFER DATA pulse width is 50 ns.

   If TRANSFER DATA is held permanently HIGH then the Counter outputs will appear directly at the bit outputs.

3. Serial output data (MSB first) can be obtained from the MSB output (Pin 27) by applying a DATA CLOCK (Pin 16, 1 MHz maximum, 100 ns minimum pulse width).

4. A LOW on SEND DATA (Pin 17) disables the DATA CLOCK and turns off all the output transistors so that all the bit outputs are HIGH (see diagram of output).

94

LOGIC CODING

Table 1. Unipolar Operation

Analogue Input Notes 1, 2	Digital Output Code MSB LSB
FS −1LSB	1111111111
FS −2LSB	1111111110
¾ FS	1100000000
½ FS +1LSB	1000000001
½ FS	1000000000
½ FS −1LSB	0111111111
¼ FS	0100000000
1LSB	0000000001
0	0000000000

Table 2. Bipolar Operation

Analogue Input Notes 1, 2	Digital Output Code MSB LSB
+(FS −1LSB)	1111111111
+(FS −2LSB)	1111111110
+(½ FS)	1100000000
+(1LSB)	1000000001
0	1000000000
−(1LSB)	0111111111
−(½ FS)	0100000000
−(FS −1LSB)	0000000001
−FS	0000000000

NOTES:

1. Analogue inputs shown are nominal centre values of code.

2. "FS" is full scale.

OFFSET AND GAIN SETTING

For unipolar, supply an input of ½LSB for transition 0000000000 to 0000000001, and of (full scale −1½LSB) for transition 1111111111 to 1111111110.

For bipolar, supply an input of −(full scale −½LSB) for transition 0000000000 to 0000000001, and of (full scale −1½LSB) for transition 1111111111 to 1111111110.

Fig. 6 – TYPICAL REFERENCE VOLTAGE v TEMPERATURE (ALL TYPES)

ZN433 Series

PIN CONNECTIONS

Pin	Signal		Pin	Signal
1	0 V		28	TRANSFER DATA
2	-5V		27	SERIAL O/P BIT 1
3	SHAPE		26	BIT 2
4	REF. AMP. GND.		25	BIT 3
5	REF. AMP. I/P		24	BIT 4
6	V_{REF} +2·48V		23	BIT 5
7	0 V		22	BIT 6
8	0 V		21	BIT 7
9	I REF		20	BIT 8
10	I OUT		19	BIT 9
11	COMP. I/P		18	BIT 10 (LSB)
12	COMP. GND.		17	SEND DATA
13	+5V		16	DATA CLOCK
14	N.C.		15	MAIN CLOCK

5475/1

CHIP DIMENSIONS AND LAYOUT

172 MIL

159 MIL

6225

96

FERRANTI
semiconductors

ZNA116E

FEATURES

● 3½ Decade display (±1999 max. reading)

● Automatic polarity detection and indication

● Leading zero suppression

● Overload indication

● Multiplexed B.C.D. outputs capable of driving a T.T.L. decoder/driver directly (e.g. ZNA7447A)

● External input to blank display

● Internal oscillator, adjustable externally

● An output at $^1/_{100}$ clock frequency for under range indication, or for synchronising the clock frequency for optimum mains rejection

● Single rail, 5 volt supply operation (at 10 mA typical)

GENERAL DESCRIPTION

The ZNA116E allows a precision 3½ digit D.V.M to be constructed very easily. It provides all the control logic necessary for a D.V.M using the well known dual slope integration technique. The low power requirements of the device make it attractive for portable battery operated applications and, since it is bipolar, requires no special handling precautions.

System Diagram

97

ZNA116E

PINNING AND FUNCTIONAL DETAILS

Pin number	Name	Function
1	Earth	Supply 0 volts
2	f/100 output	An output at $^1/_{100}$ of the clock frequency is available at this pin.
3	Clock input	An external clock can be applied at this pin, or the internal oscillator can be used by linking it to pin 14. A measurement is made every 8000 clock periods. Transfer of a number to the latches occurs at the first −VE going clock edge after comparison has been made. The counter toggles on +VE going clock edges. Max. clock frequency = 50 kHz, Min. logic 0 time at clock input = 8 μsec.
4	M1	Digit drive output. When this output is low, the most significant digit is displayed.
5	M2	Digit drive output. When this output is low, the second most significant digit is displayed.
6	M3	Digit drive output. When this output is low, the third most significant digit is displayed.
7	M4	Digit drive output. When this output is low, the least significant digit is displayed. The multiplexed frequency = $^1/_{40}$ clock frequency.
8	Blank input	When this input is held at logic 1, the data outputs, A,B,C,D, will also all be at a logic 1. This is detected by the T.T.L. decoder/driver and the display is switched off.
9	D.P. input	When this input is at logic 1, leading zeroes are blanked off. Pins 5 and 6 can be wired to the D.P. input to give the correct display, when a decimal point is displayed. (see diagrams).
10	A	2^0 BCD data output
11	B	2^1 BCD data output
12	C	2^2 BCD data output
13	D	2^3 BCD data output
14	Oscillator output	Link to pin 3 if internal oscillator is to be used.
15	Oscillator input	External components, connected to this pin, control oscillator frequency. (see figure 1).
16	+VE reference switch output	When this output is at logic 1, it connects the +VE reference voltage into the integrator.
17	−VE reference switch output	When this output is at logic 1, it connects the −VE reference voltage into the integrator.
18	−Sign output	This output is at logic 1 when a negative input voltage is being measured.

ZNA116E

PINNING AND FUNCTIONAL DETAILS

Pin number	Name	Function
19	+Sign output	This output is at logic 1 when a positive input voltage is being measured.
20	Comparator input	This input is connected to the output of the external compartaor.
21	Signal switch output	When this output goes to logic 1, it connects the voltage to be measured into the integrator.
22	V_{CC}	Supply +5 volts.
23	Reset switch output	When this output is at logic 1, the switch across the integrator capacitor is turned on to completely discharge it.
24	Overload output	If the integrator capacitor does not discharge completely until after the counter has reached 2000, this output will go to logic 1.

ZNA116E

TECHNICAL DATA

(a) Maximum Ratings:

Supply voltage ..   ..   5.5 volts
Operating temperature   ..   ..   0°C to +70°C
Storage temperature ..   ..   ..   −55°C to +125°C

(b) Electrical Characteristics ($T_A = 0°C$ to $+70°C$)

Parameter	Min.	Typ.	Max.	Units	Test conditions
Supply voltage V_{OC}	4.75		5.25	Volts	
Supply current I_{CC}			15.0	mA	$V_{CC} = 5$ volts
Logic 0 level V_{IL} All input pins except pin 15			0.8	Volts	
Logic 1 level V_{IH} All input pins except pin 15	2.0			Volts	
High-level input current I_{IH} All input pins except pin 15			4.0	μA	$V_{in} = V_{CC}$
Low-level input current All input pins I_{IL}			−4.0	μA	$V_{in} = 0V$
Logic 0 level V_{OL} Output pins 2,4,5,6,7,10, 11,12,13			0.4	Volts	$I_{sink} = 1.6$ mA
Logic 0 level V_{OL} Output pins 14,18,19,21,24			0.4	Volts	$I_{sink} = 1.0$ mA
Logic 0 level V_{OL} Output pins 16,17,23			0.4	Volts	$I_{sink} = 0.5$ mA
Logic 1 level V_{OH} All output pins except pin 14	2.4			Volts	$I_{out} = 10$ μA
Oscillator frequency		20.0		kHz	With timing components shown in figure 1
Temperature coefficient of oscillator		±0.02		% per °C	Excluding temp. coefficient of the external timing components
Variation in oscillator frequency with changes in V_{CC}		−0.4		% per volt	$T_A = 25°C$

(c) Notes:

1. Pin 14 is an open-collector output. All other outputs have a nominal 100 kΩ pull-up resistor to V_{CC} rail.
2. Although the oscillator and logic will function up to 50 kHz, this is not recommended as the analogue circuitry becomes more critical.

OSCILLATOR CIRCUIT

RECOMMENDED COMPONENTS FOR 20 kHz OPERATION
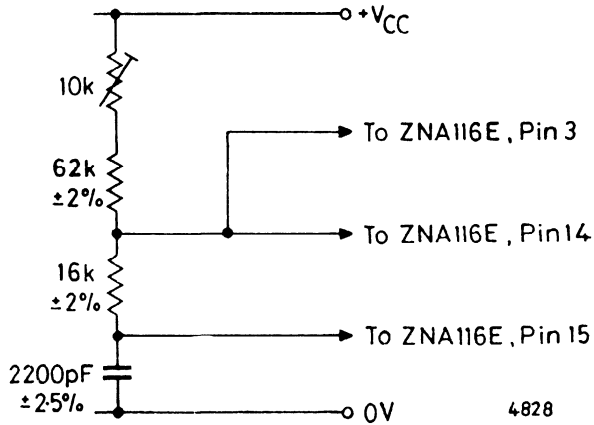
Figure 1.

Notes:

(a) Oscillator stability is better than 0.02% per °C.

(b) The potentiometer should be set so that the frequency of oscillation is 20 kHz. This is best monitored at pin 2, to avoid loading the oscillator while setting up.

(c) The potentiometer and the 62k resistor can be replaced by a single 68k $\pm$2% high stablity resistor at the loss of some mains rejection only.
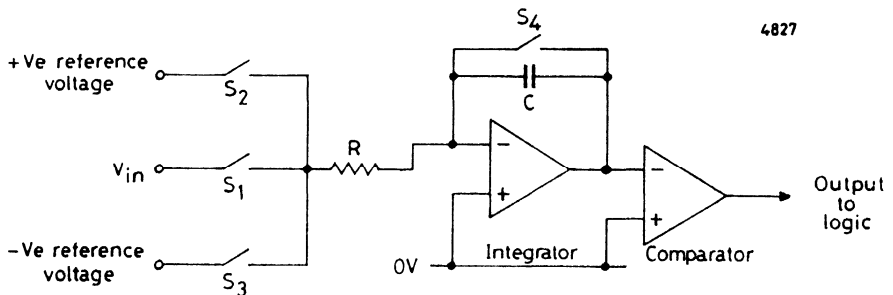

THE DUAL SLOPE SYSTEM

Figure 2.
(Refer to timing diagram, figure 3)

101

ZNA116E

At time T_1 ; S2, S3 and S4 are open and S1 closes to apply the input voltage, V_{in}, to the integrator. The integrator capacitor, C, charges up linearly until time T_2 which is 4000 clock periods after T_1. The voltage at the integrator output, V_x, at time T_2 is proportional to V_{in}.

At time T_2, S1 is opened and either S2 or S3 is closed, to apply a reference voltage, of the opposite polarity to V_{in}, to the integrator, Thus C is made to discharge at a constant rate and at time T_3 the output voltage of the integrator will again be zero. This is detected by the comparator and the reference voltage is now switched off and the number of clock pulses corresponding to T_x will be transferrred to latches and displayed. This number is proportional to V_x and hence is proportional to V_{in}. If T_x exceeds 2000 clock periods, an overload condition is indicated.

At time T_4, which is 3000 clock periods after T_2, S4 closes to completely discharge the capacitor. At time T_5, which is 4000 clock periods after T_2, S4 opens and the cycle is repeated.

If S1 is closed for a time which is a multiple of 20 msec., any 50 Hz mains ripple superimposed on V_{in} will be integrated to zero and thus good mains rejection is obtained.

The dual slope D.V.M. does not require a high stability capacitor or high stability oscillator (unlike single slope systems) to achieve high accuracy.

ZNA116E TIMING

4830

Figure 3.

102
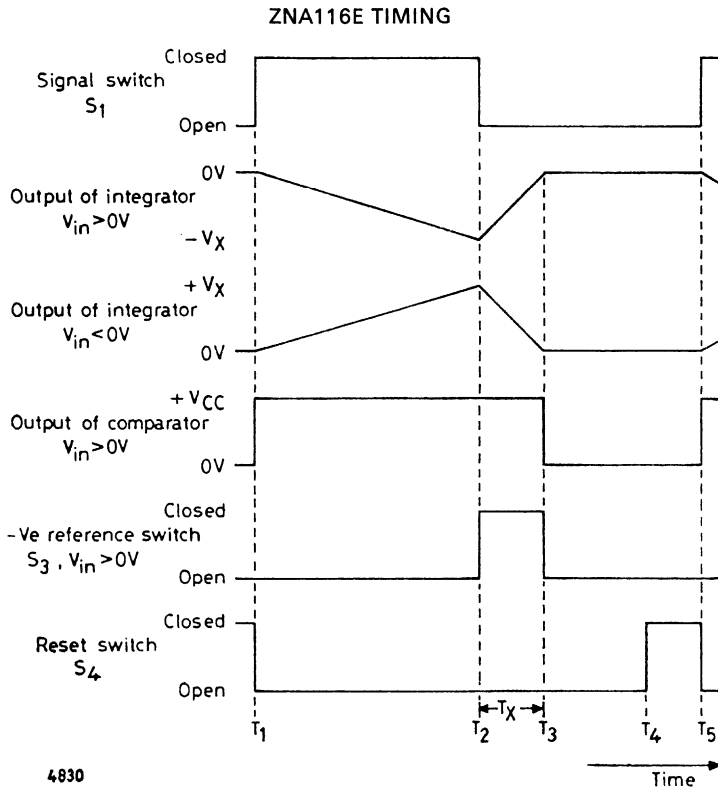
THE DESIGN OF D.V.M. CIRCUITS USING THE ZNA116E

The ZNA116E provides the control logic necessary to construct a D.V.M. with a $3\frac{1}{2}$ digit display having an accuracy of $\pm\frac{1}{2}$ digit. The actual accuracy obtained will depend on four factors:

(a) Accuracy of calibration.

(b) Stability of reference sources.

(c) Stability of transistor switches.

(d) Operational amplifier drift.

The circuit details are given for the construction of a simple D.V.M. circuit which runs off a single 5 volt supply rail. The accuracy of this D.V.M., typically 0.1% ±1 mV., (on the 1v. range) should be adequate for many applications.

To achieve this accuracy, the nominal 5 volt supply rail should be held stable to ±50 mV. An I.C. voltage regulator is ideal for this purpose.

The main factor limiting the performance of this circuit is (d). If a better performance is required, an amplifier with a lower bias current must be used (e.g. ZN741) running of ±5 volt supply rails, so that the drift becomes less significant. More elaborate interfacing with the ZNA116E will be required in this case.

D.V.M. CONSTRUCTION

Due to the clearly defined application of the ZNA116E, the full circuit is given for a simple $3\frac{1}{2}$ digit D.V.M. together with full printed circuit board details.

The construction is defined in two distinct halves an analogue board containing integrator, comparator, reference supplies and transistor switches; and a digital board containing the ZNA116E, display, driver and oscillator components. This allows the constructor the chance to alter the 'front end' (analogue circuit) if desired, without disturbing the digital board.

ZNA116E
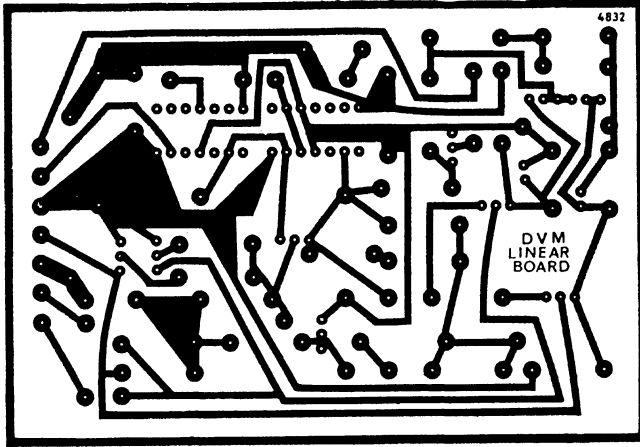
Figure 4. ANALOGUE BOARD (copper side) $\frac{3}{4}$ FULL SIZE
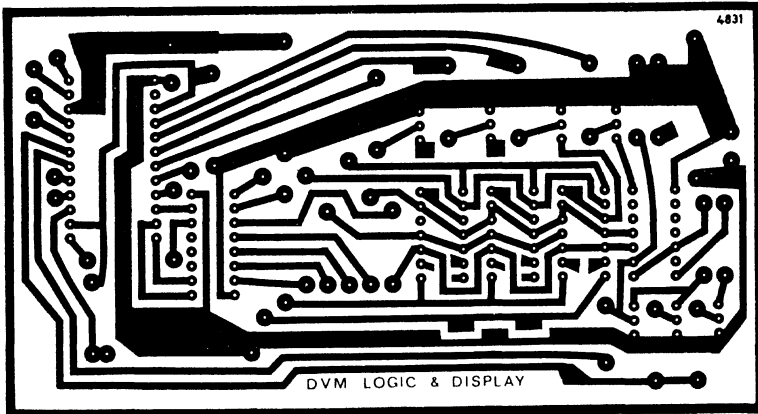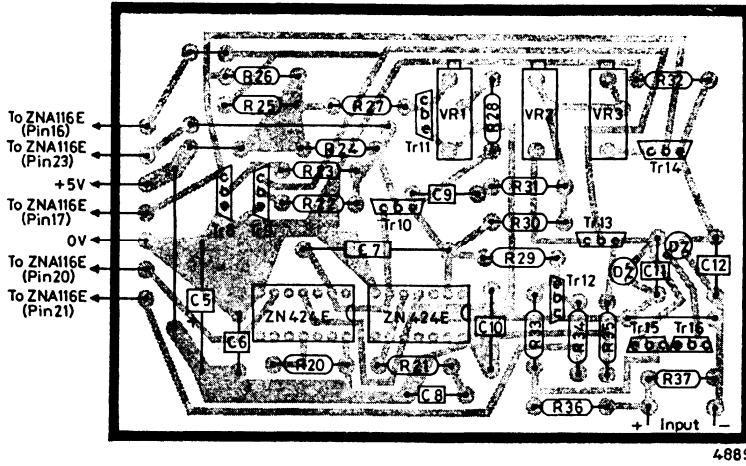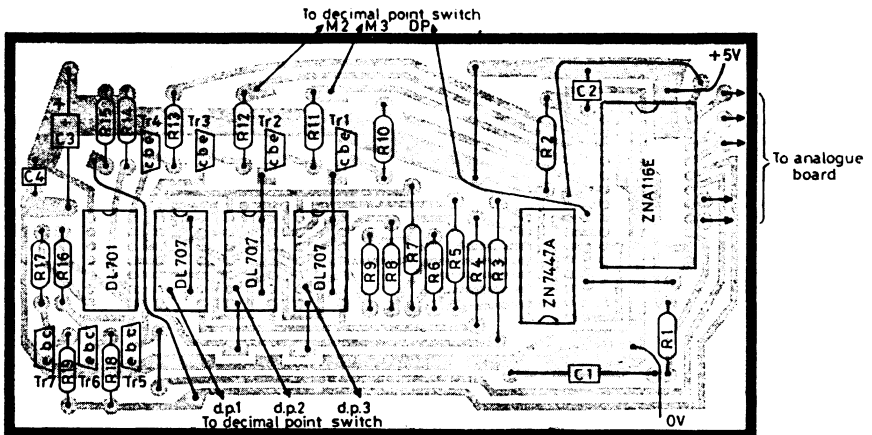

Figure 5. DIGITAL BOARD (copper side) $\frac{3}{4}$ FULL SIZE

ANALOGUE BOARD – Component positions

Figure 6.

DIGITAL BOARD – Component positions

Figure 7.

105

ZNA116E

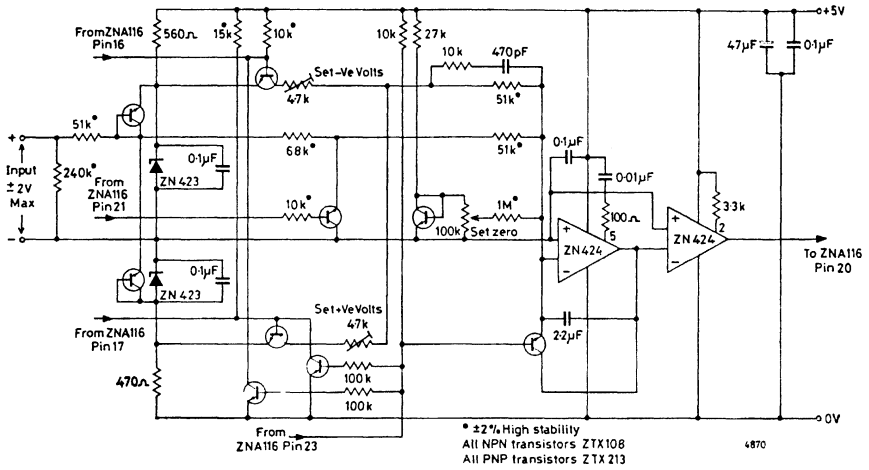## CIRCUIT DIAGRAM OF ANALOGUE BOARD
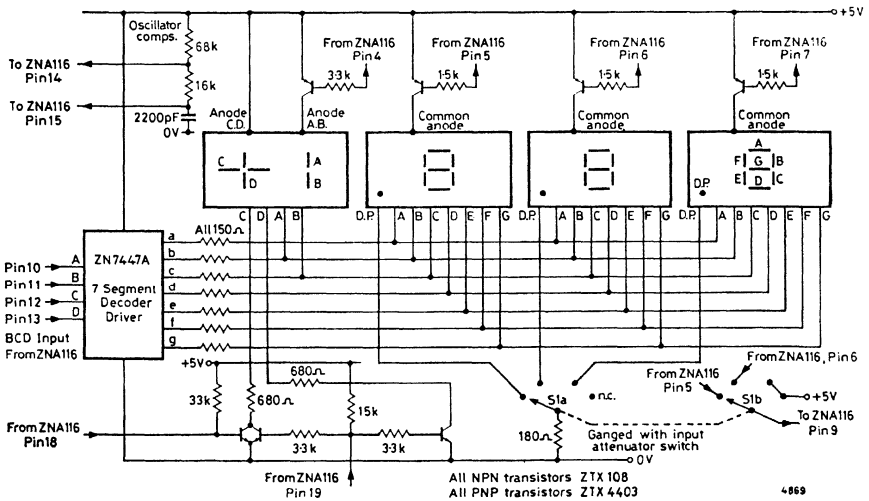

Figure 8.

CIRCUIT DIAGRAM OF DIGITAL BOARD

Figure 9.

D.V.M. COMPONENT LIST

R1	16k ±2%		R14	33k		R27	27k	
R2	68k ±2%		R15	15k		R28	1M ±2%	
R3	150		R16	680		R29	51k ±2%	
R4	150		R17	680		R30	51k ±2%	
R5	150		R18	3.3k		R31	10k	
R6	150		R19	3.3k		R32	470	
R7	150		R20	3.3k		R33	68k ±2%	
R8	150		R21	100		R34	10k ±2%	
R9	150		R22	100k		R35	560	
R10	1.5k		R23	100k		R36	51k ±2%	
R11	1.5k		R24	10k		R37	240k ±2%	
R12	1.5k		R25	10k		R38	180	
R13	3.3k		R26	15k				

VR1 100k ⎞
VR2 5k   ⎬ Bourns 3009P
VR3 5k   ⎠

All values given in ohms.

All resistors ±10% unless stated otherwise.

C1	2200 pF ±2.5%
C2	0.033 µF
C3	68 µF 10 vw. electrolytic ±50%
C4	0.033 µF
C5	68 µF 10 vw. electrolytic ±50%
C6	0.1 µF
C7	2.2 µF ±10%
C8	0.01 µF
C9	470 pF
C10	0.1 µF
C11	0.1 µF
C11	0.1 µF
C12	0.1 µF

All capacitors ±20% non-electrolytic unless stated otherwise.

Tr1, Tr2, Tr3 Tr4   all ZTX4403
Tr5, Tr6, Tr7, Tr8, Tr9, ⎞
Tr10, Tr11, Tr13 Tr14,   ⎬ all ZTX 108
Tr15, Tr16,   ⎠
Tr12   ZTX213
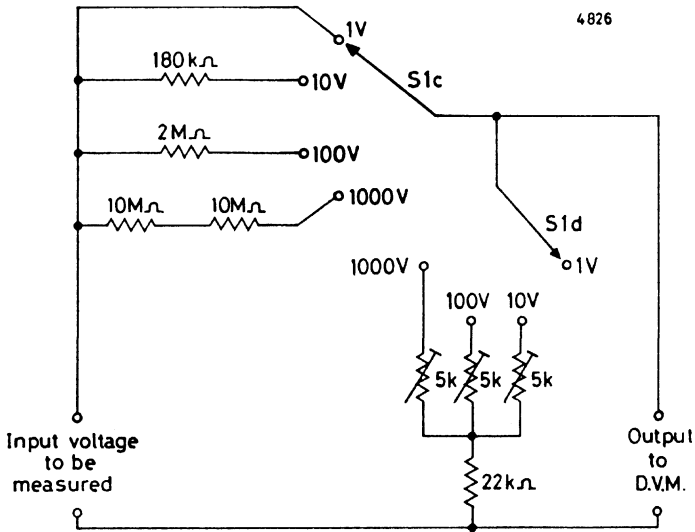
D1, D2   both ZN423

ZNA116E 1 off
ZN424E   2 off
ZN7447A 1 off

DL707L display 3 off
DL701 display 1 off

ZNA116E

ATTENUATION OF INPUT VOLTAGE

For measuring voltages of ± 2 volts or more, the following input attenuator circuit may be used.

All resistors $\pm 2\%$ high stability, presets $\pm 20\%$ carbon.

Figure 10.

The input impedance is 100 kΩ on the 1 volt range and 20 kΩ/volt on the other three ranges. If a greater impedance than this is required, an attenuator using higher value resistors followed by an F.E.T. input buffer amplifier should be used.

Note: In the above diagram, switches S1c and S1d are ganged with S1a and S1b, the decimal point switch, shown in figure 9.

CONSTRUCTIONAL NOTES

(1) The leads joining the analogue board to the digital board should not be longer than about six inches.

(2) Before connecting the circuit to a power supply, make sure that all the external links, shown in figures 6 and 7, have been connected to the printed circuit boards. There should be five links on the analogue board and twelve on the digital board.

(3) If the applied input voltage is too large, the display will be blanked off as an overload indication. If a diode is connected between pins 8, 24 and 21 of the ZNA116E, as shown below in figure 11, the display will flash for overload conditions.
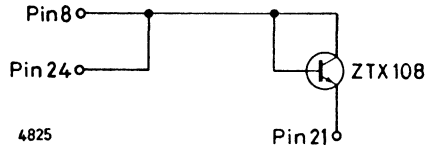
Figure 11.

CALIBRATION PROCEDURE

The range switch is placed in the 1 volt position and the input terminals are shorted together. VR2 and VR3 should be set about half-way. The set-zero preset VR1 is now adjusted until the display just flickers between +0 and −0.

A known positive voltage, between one and two volts, is now connected to the input terminals and VR3 is adjusted until this voltage is displayed.

The input voltage is then reversed and VR2 is adjusted until the display is again correct.

VR1, VR2 and VR3 are now correctly set and should not need altering again.

Since the three 5k presets in the attenuator section are completely independent of each other, these can be easily set to give the required attenuation of 10, 100 and 1000.

Calibration is now complete.

SPECIFICATION OF D.V.M.

Maximum reading	± 1999
Readings per second	$2\frac{1}{2}$ typical
Typical accuracy (1 volt range)	0.1% of reading ± 1 mV
Temperature coefficient (1 volt range)	± 0.1 mV per °C typical
Input impedance	100 kΩ for 1 volt range 200 kΩ for 10 volt range 2 MΩ for 100 volt range 20 MΩ for 1000 volt range
Total supply current (with all segments on)	200 mA typical

ZNA116E

PIN CONNECTIONS

GND 1	24 OVERANGE
F/100 2	23 RESET SW
CLOCK 3	22 V_{CC}
M1 4	21 SIGNAL SW
M2 5	20 COMP IN
M3 6	19 +SIGN
M4 7	18 −SIGN
BLANK 8	17 −REF. SW.
D.P. 9	16 +REF. SW.
A 10	15 OSC. IN
B 11	14 OSC. OUT
C 12	13 D

6235

CHIP DIMENSIONS AND LAYOUT

145 MIL

DP   BLANK   M4 M3   M2 M1

A

B — CLOCK INPUT

C — F/100

D

143 MIL

OSC. I/P — OVERRANGE OUTPUT

OSC. O/P — RESET OUTPUT

6226

REF +   REF −   −SIGN   +SIGN   COMP. INPUT   SIG. SW.O/P

FERRANTI semiconductors

ZNA216E
ZNA216J
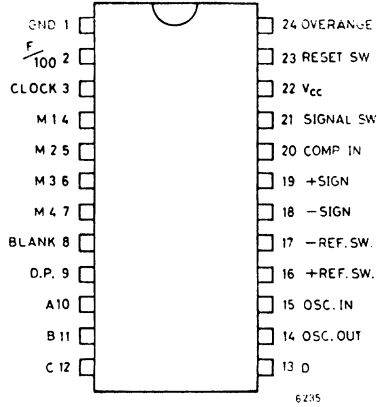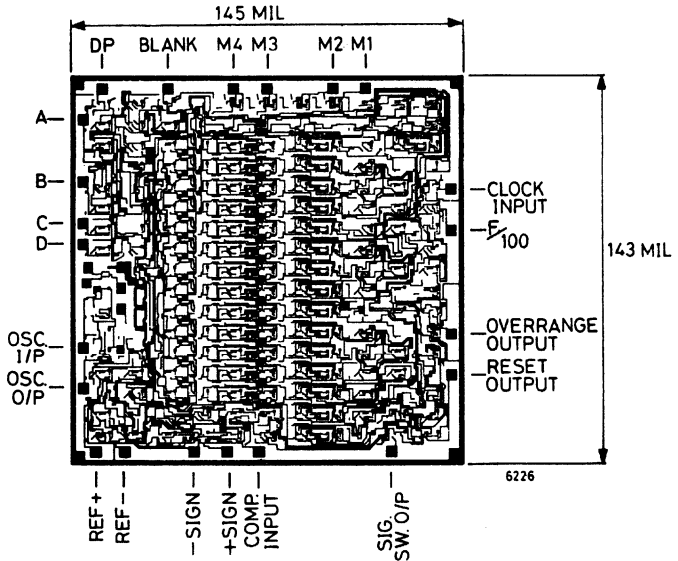
FEATURES

- 3½ digit display (±3999 max. reading)
- Automatic zero adjustment with 1 µV/°C temperature coefficient
- Seven-segment outputs for direct drive of LED displays
- BCD outputs
- Automatic polarity detection and indication
- Flashing overload indication, separate overload output
- Blanking input, e.g. for low battery indication
- Automatic blanking of display leading zeroes
- On-chip clock, may be externally synchronised
- TTL and CMOS compatible
- Single +5V supply
- Pinning optimised for easy p.c.b. layout

DESCRIPTION

The ZNA216 D.V.M. I.C. is a versatile D.V.M. system component which contains all the control logic necessary to construct a dual-slope digital voltmeter, whilst leaving the designer free to configure the analogue circuitry to his own requirements.

The I.C. has multiplexed data outputs, both in BCD format and in seven-segment format for direct drive of LED displays. A number of useful features are incorporated into the device, including leading zero blanking of the display, flashing over range indication and an auto zero facility which removes the need for manual zero adjustment.

Apart from the more obvious applications of D.V.M. and D.P.M. the I. C. can be used to construct any other instrument where an analogue input from, say, a transducer is to be converted into a digital reading, for example a digital thermometer. The ZNA216 may also be used as an A-D converter in single-channel data acquisition systems, or to interface to a microprocessor system.

System Diagram

111
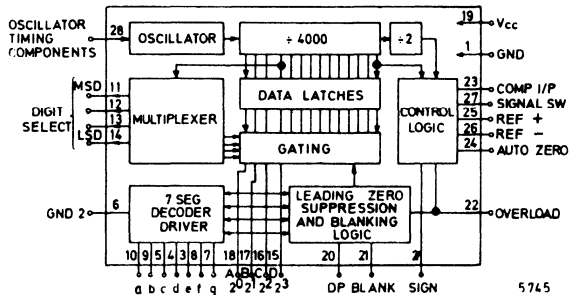
ZNA216E/J

Pin number	Name	Function
1	Gnd 1	Supply 0 volts
2	Sign	Open collector output, goes low when −ve input voltage is being measured.
3	e	Open collector segment output, goes low when segment is on.
4	d	Segment output as above.
5	c	Segment output as above
6	Gnd 2	0 volt supply for segment drivers, must be connected to Pin 1.
7	g	Segment output as above
8	f	Segment output as above
9	b	Segment output as above.
10	a	Segment output as above
11	M1	Digit drive output, goes low for the most significant digit to be displayed, first in digit scan sequence.
12	M2	Digit drive output, goes low for the second most significant digit fo be displayed, second in digit scan sequence.
13	M3	Digit drive output, goes low for the third most significant digit to be displayed, third in digit scan sequence.
14	M4	Digit drive output, goes low for the least significant digit to be displayed, fourth in digit scan sequence.
15	D	2^3 BCD data output.
16	C	2^2 BCD data output.
17	B	2^1 BCD data output.
18	A	2^0 BCD data output.
19	V_{CC}	Supply +5 volts.
20	DP	When this input is at logic 1, leading zeroes are blanked.
21	Blank	While this input is at logic 1, all segment outputs are off and all BCD data outputs are at logic 1.
22	Overload	If the integrator capacitor does not discharge before the conter reaches 4000, this output goes to logic 1.
23	Comp.	This input is connected to the output of the external comparator.
24	Azero	When this output is high, auto zero correction is applied to the integrator.

Pin number	Name	Function
25	Ref+	When this output is at logic 1, the +ve reference voltage is connected to the integrator.
26	Ref–	When this output is at logic 1, –ve reference voltage is connected to the integrator.
27	Signal switch	When this output is at logic 1, the input voltage to be measured is connected into the integrator.
28	Clock	The external clock oscillator components are connected to this pin (see diagrams). Alternatively, this pin may be driven by an external signal. A measurement is made every 8000 clock periods. The counter toggles on –ve going clock edges and transfer to the latches occurs at the first +ve going clock edge after comparison has been made which avoids false triggering from the integrator output. Max. clock frequency 50 kHz.

ZNA216E/J

(a)   Absolute Maximum Ratings:

Supply voltage	7.0 volts
Operating temperature	0°C to +70°C
Storage temperature	−55°C to +125°C

(b)   Electrical Characteristics ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V$ unless otherwise specified).

Parameter		Min.	Typ.	Max.	Unit	Test conditions
Supply voltage		4.5		5.5	V	
Supply current				20	mA	
Low level input voltage	All inputs			0.8	V	
Low level input current	All inputs			−4	μA	$V_{in} = 0V$
Input clamp diode voltage	All inputs			−1.5 V_{CC} +1.5	V V	$I_{in} = -12$ mA $I_{in} = 10$ mA
High level input voltage	Oscillator RC input	2.5			V	
	All other inputs	2.0			V	
High level input current	Oscillator RC input			100	μA	$V_{in} = 2.5V$
	All other inputs			4	μA	$V_{in} = 5.0V$
Low level output voltage	a, b, c, d, e, f, g			0.8	V	$I_{sink} = 20$ mA
	Sign			0.4	V	$I_{sink} = 5$ mA
	Overload, Ref+, Ref−, Azero, Signal switch, a,b,c,d,M1,M2, M3, M4			0.4	V	$I_{sink} = 1.6$ mA
High level output voltage	Overload, Ref+, Ref−, Azero, Signal switch, a,b,c,d,M1,M2, M3, M4	2.4			V	$I_{out} = 10$ μA
			V_{CC} −0.1		V	$I_{out} = 0$
High level output current	a,b,c,d,e,f,g Sign			−10	μA	$V_{out} = 5.0V$

(c)   Note:

Although the oscillator and logic will function up to 50 kHz, this is not recommended as the analogue circuitry becomes more critical.
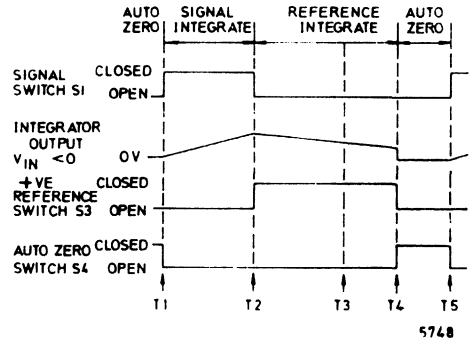
114

THE DUAL SLOPE SYSTEM
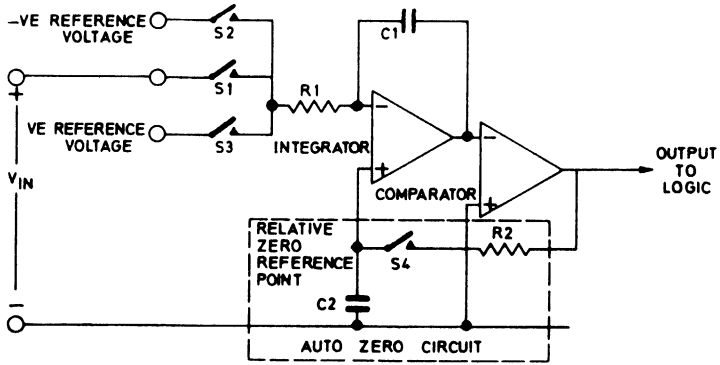
Figure 1. Dual Slope Block Diagram.

5746
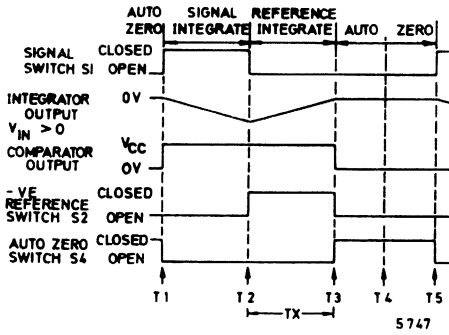
5747

Figure 2a. Timing Diagram for in-range input.

5748

Figure 2b. Timing diagram for overrange input

115

ZNA216E/J

Dual slope integration is a D.V.M. circuit technique designed to cancel out the effects of drift in circuit components. A block diagram of the analogue section of a dual-slope D.V.M. is shown in figure 1, whilst a timing diagram for its operation is shown in figure 2.

At time T_1, S1 is closed by the D.V.M. logic, connecting the input signal to the integrator until time T_2, which is 2000 clock periods after T_1. During this time the integrator output ramps positive or negative, depending on input voltage polarity, to a voltage

$$V_o = \frac{-V_{in}\, 2000\, t_c}{R_1 C_1}$$

where t_c is the clock period.

The polarity of the integrator output voltage during this period, and hence of the input voltage, is sensed by the comparator, whose output is connected to the control logic.

At time T_2, S1 is opened and, depending on the input voltage polarity, either S2 or S3 is closed. This connects a reference voltage of opposite polarity to V_{in} to the integrator input, so that the integrator output ramps back towards zero. The number of clock periods required for the integrator output to reach zero is counted by the DVM counter. When the output reaches zero the comparator output changes state, S2 or S3 opens and the count is stopped. Since the second integration also takes place over a voltage V_o then,

$$V_o = \frac{-V_{REF}\, n t_c}{R_1 C_1} \quad \text{where n is the count at time } T_3$$

but V_o also equals $\dfrac{-V_{in}\, 2000 t_c}{R_1 C_1}$

thus $n = \dfrac{2000\, V_{in}}{V_{REF}}$

R_1, C_1 and t_c have disappeared from this final equation, so the accuracy of the D.V.M. is unaffected by the long-term stability of these parameters. The only factors influencing accuracy are the stability of V_{REF} and variations in the 'on' resistance of the analogue switches S1 to S3. The former can be assured by careful choice of a reference source, e.g. the Ferranti ZN423 or ZN458, whilst the effect of the latter can be minimised by making R_1 lage compared to the on resistance of S1 to S3.

If V_{REF} is exactly 2V then n = 1000 V_{in}, i.e. the count will be equal to the input voltage in millivolts. For the ZNA216 the maximum reading is 3999. If a count of 4000 occurs before the integrator output reaches zero, as shown in figure 2b, then S2 or S3 will open and the overrange output will go high.

In a practical D.V.M. it is unlikely that a reference voltage of exactly 2V will be available, or an input range other than 3.999V may be required. In this case a different resistor value (R_{REF}) will be used for the reference integration. The equation then becomes :

$$n = \frac{2000\, V_{in} \cdot R_{REF}}{V_{REF} \cdot R_1}$$

R_1 and R_{REF} should be high-stability types.

AUTO ZERO

Any offset voltage and bias current in the integrator will be integrated along with the input signal and since, for example, a 3.999V D.V.M. has a resolution of 1 mV an offset of a few hundred microvolts can lead to errors in the least significant digit. Manual zero adjustment is time-consuming and has to be repeated frequently due to temperature drift.

The auto zero of the ZNA216 operates during the period T_3 to T_5, or T_4 to T_5 in the case of an overrange input. S4 is closed, S1 S2 and S3 are opened so that only the integrator offset voltage is integrated, thus causing the integrator output to drift either positive or negative. The integrator output is amplified by the comparator (which is nothing more than an extremely high gain amplifier) and this charges C2 via R2 to apply a voltage to the non-inverting input of the integrator. The polarity of this voltage is such as to null out the effects of integrator offset voltage and bias current and thus cancel integrator drift. Depending on comparator gain a zero error of a few hundred nanovolts may be achieved by this method.

116

HUM REJECTION

Any mains hum pickup superimposed on the input signal will cause errors in the D.V.M. reading. However, if the period $T_2 - T_1$ is made a multiple of the mains period then equal numbers of positive and negative half-cycles of the mains waveform will be integrated and will cancel each other out. For 50 Hz mains $T_2 - T_1$ should be 20 ms or a multiple thereof, while for 60 Hz mains $T_2 - T_1$ should be 16.67 ms or a multiple thereof.

Adjustment of the period $T_2 - T_1$ is achieved by varying the frequency of the clock oscillator which controls the operation of the D.V.M.

DISPLAY MULTIPLEXING

The BCD and seven-segment data outputs are multiplexed, the data appearing in the sequence MSD to LSD. To identify which digit is present at the outputs at any time the four digit select outputs go low in turn, synchronous with the relevant digit appearing at the data outputs. The seven segment outputs can be used to drive the cathodes of a multiplexed common-anode LED display whilst the digit select outputs may be used to turn on digit-drive transistors, which activate each display digit in sequence.

DECIMAL POINT (ZERO BLANKING) INPUT

Before the start of each multiplex cycle a latch in the I.C. is set. This holds the display blanked until non-zero data appears at the BCD outputs, when the latch is reset and the disply is unblanked. For example, if the MSD were non-zero the latch could reset immediately the MSD appeared, so all four digits would be displayed. Conversely if the MSD were zero but the second digit were non-zero then the display would be blanked for the MSD and only three digits would appear. In this way leading zeroes in the display are suppressed. The LSD is always displayed whether zero or not.

The D.P. input can be used to override the zero blanking by taking this pin to logic '0'. This facility allows a correct display to be obtained when a decimal point is used.

For example, if the decimal point is to the left of the MSD then a low-going pulse to the D.P. input synchronous with the MSD output will cause all digits to the right of the decimal point to be displayed, whether zero or not. Thus, if the input voltage were, say .0056 volts then the display would be .0056. If the zero blanking were not overridden In this way the display would be .--56, which is clearly unsatisfactory.

OSCILLATOR CIRCUIT

The operation of the D.V.M. circuit is controlled by a clock oscillator, which provides drive for the counter, control logic and display multiplexing. Two external components, a resistor and a capacitor, are required to make the oscillator function. The oscillator temperature stability is typically $\pm 0.02\%$ per °C.

As mentioned earlier, the oscillator frequency should be chosen so that $T_2 - T_1$ is a multiple of the mains period. It should not be chosen so low as to cause noticeable flicker in the display multiplexing, but on the other hand it should not be chosen too high or the design of the analogue circuitry becomes more critical.

The optimum oscillator frequency is 20 kHz since this makes $T_2 - T_1 = 100$ ms which gives good hum rejection at either 50 Hz or 60 Hz. This frequency can be obtained by using the component values shown in figure 3. The potentiometer may be adjusted to give a frequency of 20 kHz measured at pin 28, in which case a high impedance, low capacitance probe should be used to avoid loading the oscillator. Alternatively, the trimmer may be adjusted to give a frequency of 500 Hz at any of the digit select outputs, when no special precautions are required.

If required the oscillator timing components may be omitted and the oscillator input may be driven by an external clock at TTL logic levels.

ZNA216E/J
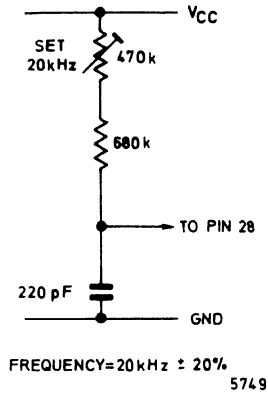

FREQUENCY=20kHz ± 20%

5749

Figure 3.   Oscillator external components.

INPUT AND OUTPUT CIRCUITS

Apart from the oscillator input (which is a Schmitt trigger type of circuit) all other inputs are as shown in figure 4a. All outputs are as shown in figure 4b, except for those designated as open-collector, which have no pull-up resistor.
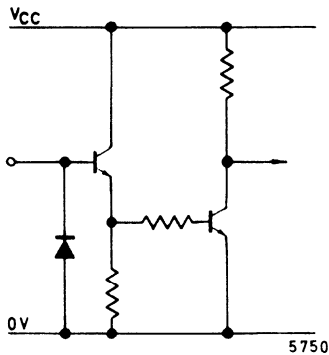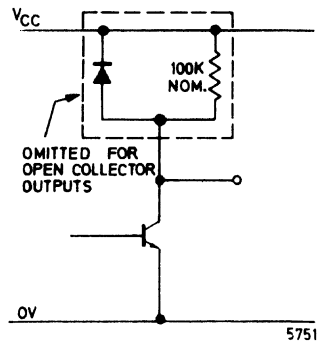

Figure 4a.   Input circuit

Figure 4b.   Output circuit

118

DISPLAY DRIVING

The 20 mA sink capability of the segment outputs allows common anode LED displays to be driven with a minimum of external components, as shown in figure 5. The segment current limit resistors should be chosen to give the desired segment current, allowing for the forward voltage drop of the LED, whilst the digit output resistors should be chosen to give sufficient base current to saturate the digit drive transistors.
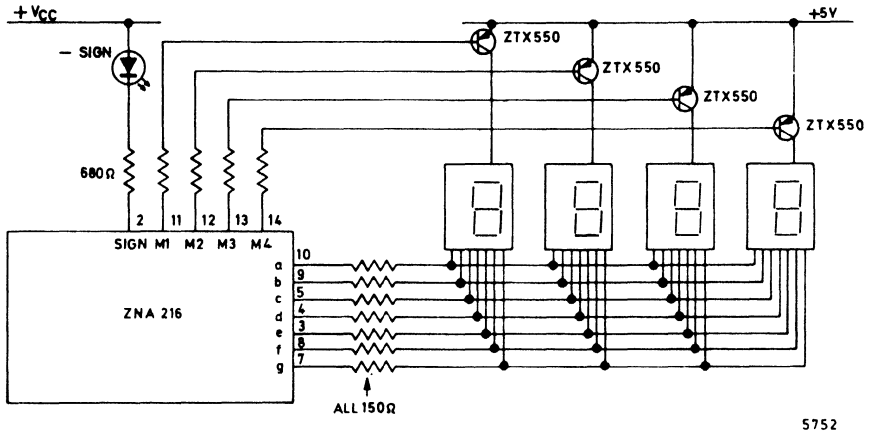
Figure 5. Display drive circuit

OVERRANGE AND LOW BATTERY INDICATION

If the input voltage exceeds the full-scale range then the display will flash all 'eights' and the over-range output, pin 22, will go high. Low battery indication may also be provided by the addition of the simple circuit shown in figure 6.

Whilst the battery voltage is above 4.4V T_1 will be turned on via R1 and R2. Below this volage the base potential supplied by these resistors will be insufficient to turn on T_1 and it will then be turned on and off cyclically by the auto-zero output, causing the display to flash whatever reading is present.
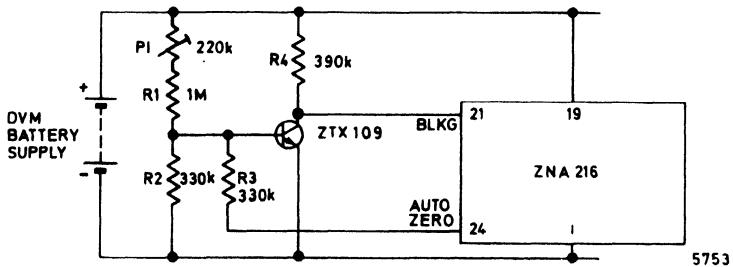
Figure 6. Low battery indication

119

ZNA216E/J

A PORTABLE D.V.M.

Figure 7 shows the circuit of a battery-powered D.V.M. based on the ZNA216, which uses readily available components. ZN424 op-amps are used for the integrator and comparator, whilst bipolar silicon transistors are used for the analogue switches. The basic sensitivity of the instrument is 4V, and additional ranges of 40V and 400V are provided by means of an input attenuator. Printed circuit board and component layouts for the D.V.M. are given in figures 8a to 9b.

However, this circuit design should by no means be considered as immutable. Since the analogue circuitry is external to the ZNA216 it may be configured to suit the designer's needs to give higher input impedance, increased sensitivity etc.

Sla & Slb Ganged With Input Attenuator Slc & Sld
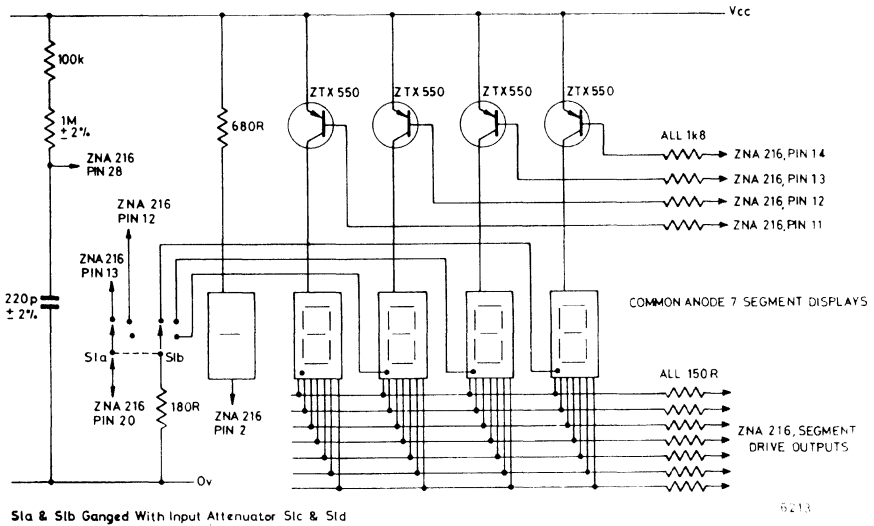
Figure 7a.   Battery-powered D.V.M. circuit, display section.

Figure 7b. Battery-powered D.V.M. circuit, analogue section.
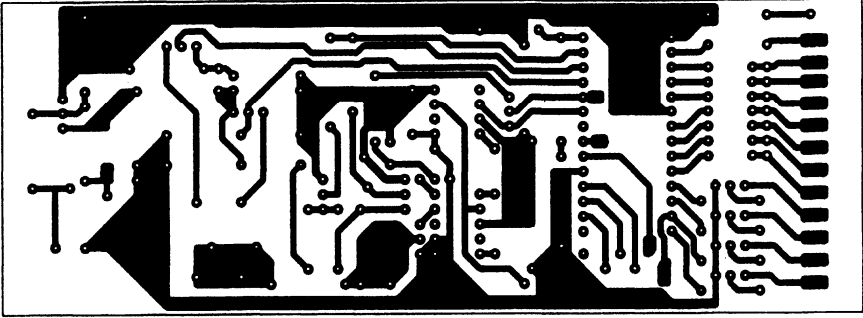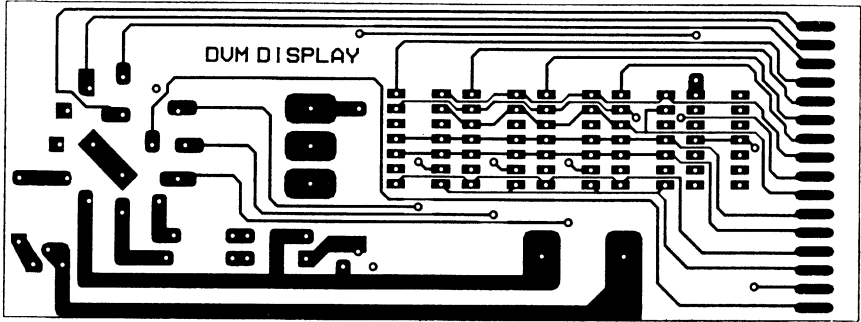
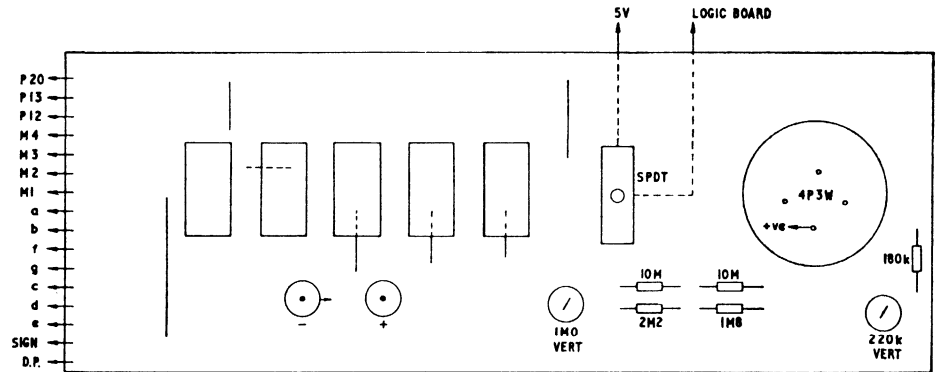# ZNA216E/J

6216

Figure 8a. D.V.M. Main Board
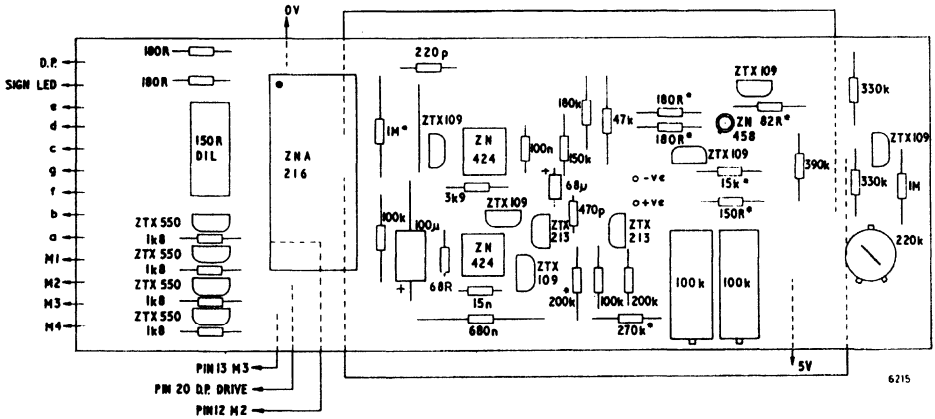
Figure 8b. Component Layout for Figure 8a.

122

6218

Figure 9a   D.V.M. Display Board

6217

Figure 9b.   Component Layout for Figure 9a.

ZNA216E/J

MICROPROCESSOR INTERFACING

The ZNA216 may be used as a dual-slope A to D converter in data loggers and other data acquisiton systems, where its $3\frac{3}{4}$ decade range offers a resolution comparable to a 13 bit binary ADC, but in a more convenient BCD format.

Figure 10 is a block diagram which illustrates how the ZNA216 may be interfaced to an 8-bit microprocessor. The principle of operation is that the four multiplexed BCD digits of the ZNA216, plus the sign and overrange bits, are stored in four 4-bit latches so that they are available in parallel form. The contents of the latches can then be read into the microprocessor as two 8-bit words. The latches used are type 74173 which have three-state outputs for direct connection to the µP data bus. Data is clocked into the latches using the positive-going edge of the appropriate digit drive outputs.

The latches are treated as two memory locations by using an address decoder which is connected to their output enable pins. In this way data can be read out of the latches just as from any other memory locations. Once data is in the latches it may be read out whilst the ZNA216 performs the next measurement, thus eliminating any waiting time. The only time when data cannot be read out of the latches is just after the ZNA216 has completed a measurement. At this time the data in the internal latches of the ZNA216 will have been updated and the data in the 74173s may thus be changing. The data in the latches will be stable after two multiplexed cycles of the ZNA216, which is 4 ms if a 20 kHz clock is used.

Since the auto-zero output of the ZNA216 goes high when a measurement has been completed this output may be used as a BUSY signal. Data should not be read from the 74173 latches until at least 4 ms after the auto-zero output has gone high.
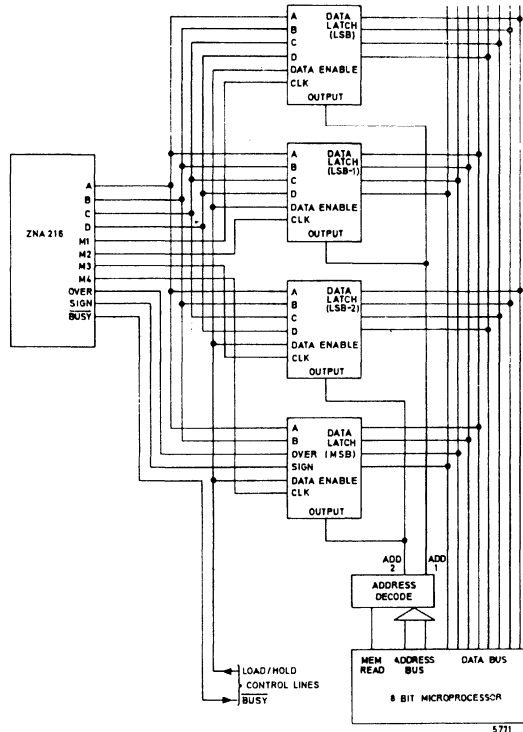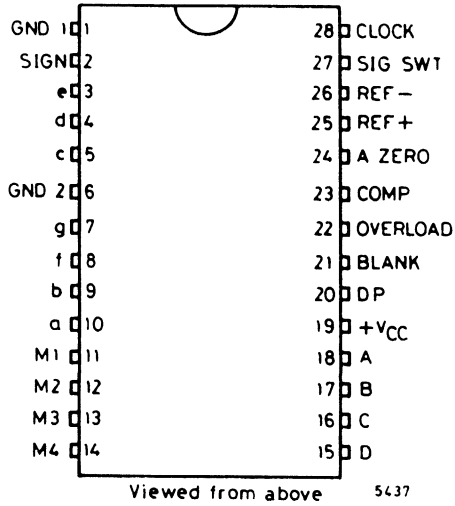

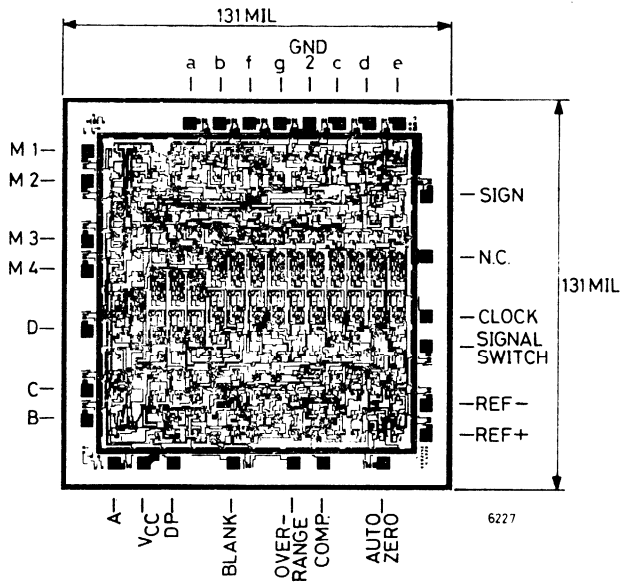Figure 10. Interfacing the ZNA216 to a Microprocessor

124

ZNA216E/J

PIN CONNECTIONS

Left	Pin		Pin	Right
GND 1	1		28	CLOCK
SIGN	2		27	SIG SWT
e	3		26	REF −
d	4		25	REF +
c	5		24	A ZERO
GND 2	6		23	COMP
g	7		22	OVERLOAD
f	8		21	BLANK
b	9		20	D P
a	10		19	+V_{CC}
M1	11		18	A
M2	12		17	B
M3	13		16	C
M4	14		15	D

Viewed from above   5437

CHIP DIMENSIONS AND LAYOUT

131 MIL

GND
a b f g 2 c d e

M 1, M 2, M 3, M 4, D, C, B

SIGN, N.C., CLOCK, SIGNAL SWITCH, REF −, REF +

A, V_{CC}, DP, BLANK, OVER-RANGE, COMP, AUTO ZERO

131 MIL   6227

125

FERRANTI semiconductors

ZNPCM1

FEATURES

● Converts a delta-sigma modulated digital pulse stream into compressed 'A' law pcm and vice-versa.

● Enables realisation of a single channel codec circuit with minimum component usage.

● Pin selectable input/output interface providing either single channel operation at 64K bit/s (2,048 kHz external clock) or up to 2,048K bit/s (2,048 kHz external clock) for multi-channel burst format.

● Encoder and decoder can be clocked asynchronously (useful for pcm multiplex applications).

● Optional alternate digit inversion.

● Electrically and pin compatible with AY-3-9900.

● Fully TTL compatible.

● Requires only a single 5V supply.

24-lead D.I.L.
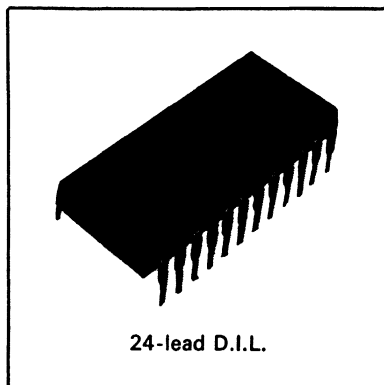
DESCRIPTION

The ZNPCM1 integrated circuit is the result of a joint development programme between the British Post Office and Ferranti Electronics Limited. Designed for use in single channel codec systems the device accepts a delta-sigma modulated pulse stream at 2,048 kHz external clock) and converts it into 8K sample/s compressed 'A' law pcm. In the decode direction the device performs the reverse function. A flexible serial pcm input/output interface is provided allowing operation in a single channel mode at 64K bit/s or at up to 2,048K bit/s (2,048 kHz external clock) for a multi-channel burst format. Digit delay control is provided to compensate for transmission delays. Optional alternate digit inversion is provided and the encoder and decoder can be clocked asynchronously if required for use in pcm multiplex applications.

Designed for use with a 2,048 kHz system clock, when operated with the required delta-sigma modulator and demodulator (see application report 'a single channel codec') The device performance complies with B.P.O. specification RC5549B and CCITT recommendations G711/G712 (1972).

The ZNPCM1 is guaranteed to operate up to 2,048 kHz and will typically operate up to 4 MHz. Operation is from a single 5V power supply with a typical power dissipation of 400 mW. All inputs and outputs are TTL compatible. Available in either a 24-lead ceramic (ZNPCM1J) or moulded (ZNPCM1CE) dual in-line package, the device is designed to operate over the temperature range 0°C to +70°C.

ZNPCM1

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	..	..	..	.. +7 Volts
Input Voltage, V_{IN}	..	..	..	.. +5.5 Volts
Operating Temperature Range			..	0°C to +70°C
Storage Temperature Range		..	..	-65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Min.	Nom.	Max.	Unit
Supply Voltage, V_{CC}	4.75	5.0	5.25	V
High-level Output Current, I_{OH}	—	—	-400	µA
Low-level Output Current, I_{OL}	—	—	4	mA
Operating Temperature Range, T_{amb}	0	—	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating temperature range).

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	High level input voltage		2.5	—	—	V
V_{IL}	Low level input voltage		—	—	0.8	V
V_{OH}	High level output voltage	V_{CC} = Min., I_{OH} = Max.	2.4	3.5	—	V
V_{OL}	Low level output voltage	V_{CC} = Min., I_{OL} = Max.	—	—	0.4	V
I_{IH}	High level input current	V_{CC} = Max., V_{IH} = Min.	—	0.2	0.4	mA
I_{IL}	Low level input current	V_{CC} = Max., V_{IL} = Max.	—	-1	-10	µA
I_{CC}	Supply current	V_{CC} = Max.	—	80	110	mA
t_{vw}	Encoder timing vector pulse width		—	488	—	ns
t_{vv}	Encoding timing vector pulse width with edge variation		—	—	100	ns
t_{ww}	Decoder timing waveform pulse width		10	15.6	—	µs
f_{max}	Operating frequency		2.048	4	—	MHz
t_r & t_f	Rise and fall times	0.4V to 3V Transition	5	––	40	ns
t_{pw}	Pulse width	Between 1.5V levels	200	—	—	ns
C_I	Input capacitance		—	—	10	pF

ZNPCM1

PIN CONFIGURATIONS

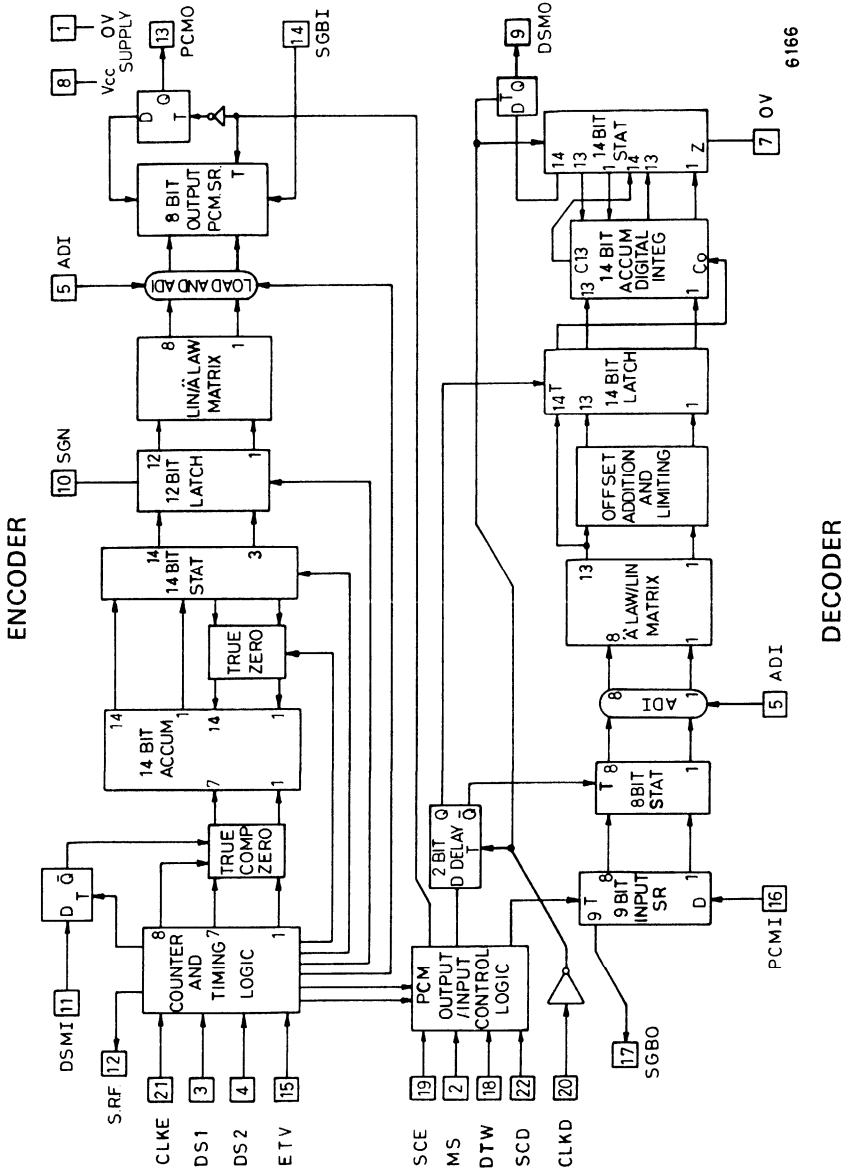| Pin	Notation	Comments
1	0V	
2	MS	MODE SELECT (Note 1) Logic 0 = External pcm I/O interface timing Logic 1 = Internal pcm I/O interface timing
3	DS1	DECODER SELECT 1 and 2 (Note 2)
4	DS2	A two bit binary word selects required digit delay between encoder and decoder. DS1 DS2 Digit Delay 0 0 0 0 1 1 1 0 2 1 1 3
5	ADI	ALTERNATE DIGIT INVERSION Logic 0 = No. ADI Logic 1 = ADI
6	N.C.	NO CONNECTION
7	0V	
8	V_{CC}	
9	DSMO	DELTA-SIGMA MODULATED OUTPUT SIGNAL
10	SGN	SIGN BIT OUTPUT Sign bit from the encoder, used to operate on the delta-sigma modulator to reduce d.c. offset effects.
11	DSMI	DELTA-SIGMA MODULATED INPUT
12	SRF	SPECTRAL REDISTRIBUTION FUNCTION Output signal used to operate on the delta-sigma modulator to reduce low frequency quantisation noise.
13	PCMO	PCM OUTPUT
14	SGBI	SIGNALLING BIT INPUT Facility for adding signalling bit(s) to the output pcm stream.
15	ETV	ENCODER TIMING VECTOR A pulse defining the beginning of each frame used to maintain encoder timing.
16	PCMI	PCM INPUT
17	SGBO	SIGNALLING BIT OUTPUT Serial output for extracting signalling bit(s) from the incoming pcm stream.

ZNPCM1

PIN CONFIGURATIONS *(continued)*

Pin	Notation	Comments
18	DTW	**DECODER TIMING WAVEFORM** A pulse used to indicate to the decoder when the input pcm stream is in the input register (required only when external shift clocks are used).
19	SCE	**ENCODER SHIFT CLOCK** Used to control the output of serial pcm data from the encoder (when MS is low).
20	CLKD	**DECODER MAIN CLOCK**
21	CLKE	**ENCODER MAIN CLOCK**
22	SCD	**DECODER SHIFT CLOCK** Used to control the input of the serial pcm data to the decoder (when MS is low).
23	N.C.	**NO CONNECTION**
24	I.C.	**INTERNAL CONNECTION** Make no external connection to this pin.

Notes:

1. With MS low (logic 0) serial PCM transmission is under the control of an externally generated shift clock SCE which can vary from 64 kHz to 2,048 kHz. The timing of this input function allows the insertion of a number of signalling bits into the PCM stream via the SGB1 input. In the high (logic 1) state the 8 bit PCM codeword will be transmitted at a rate of 64K bit/sec and each codeword will occupy the full 125 µs frame period with the leading edge of the first bit occurring at a time defined by the ETV pulse.

2. Delays through the transmission network, normally under the control of transmission switches, may cause the decoder input pulse stream to be delayed in time by a number of digits from the original transmitted pulse. To compensate for this delay two control inputs, DS1 and DS2, are provided. Consequently when MS is in the high state discrete digit delays of 0 to 3 periods may be selected resulting in a controlled shift of decoder timing in order to re-align Bit 1 in its correct position in the input register.

   When using an externally generated clock (i.e. MS in low state) an input shift clock (SCD) and timing waveform (DTW) are required to ensure that Bit 1 of the input codeword occupies its correct position in the input shift register.
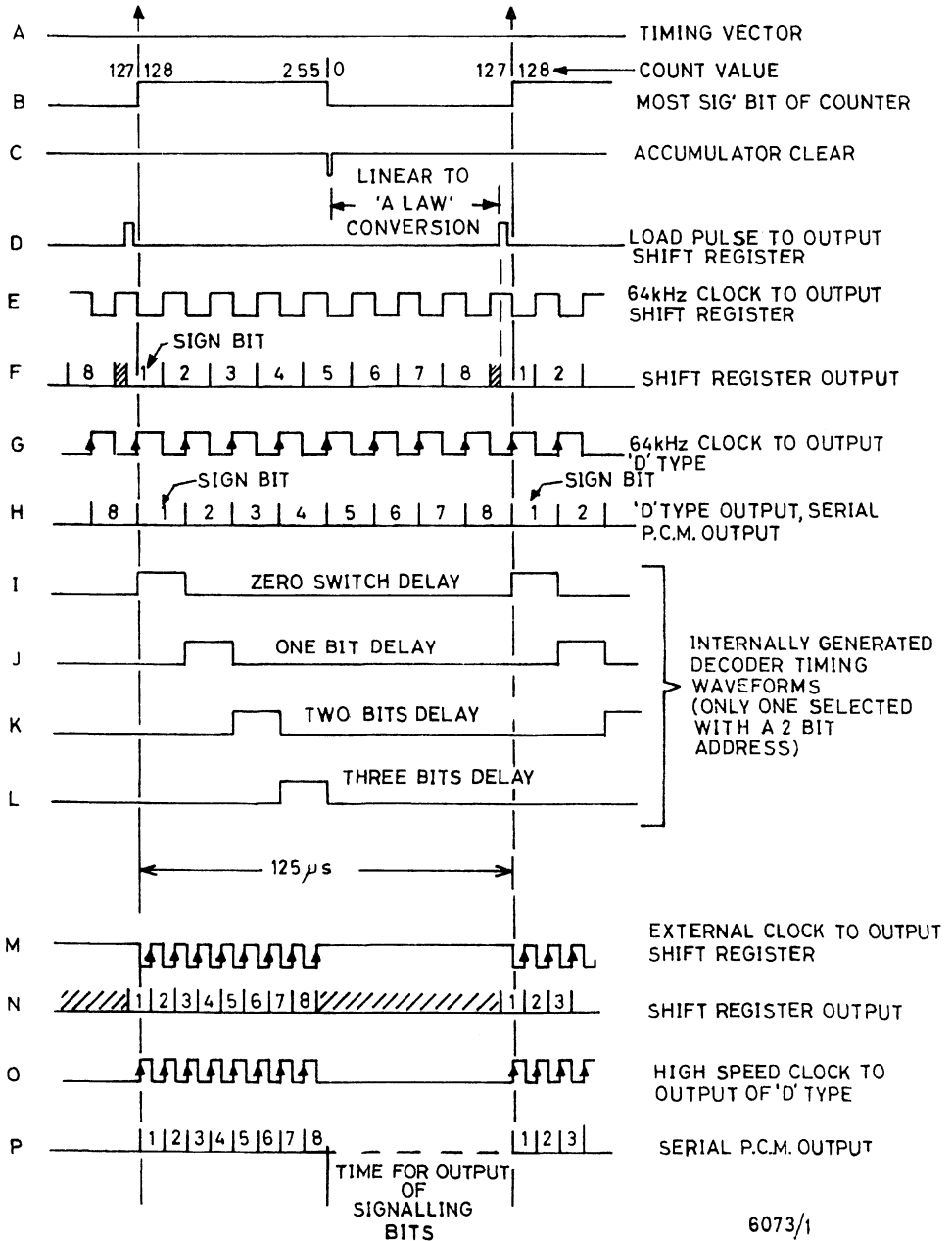
ZNPCM1
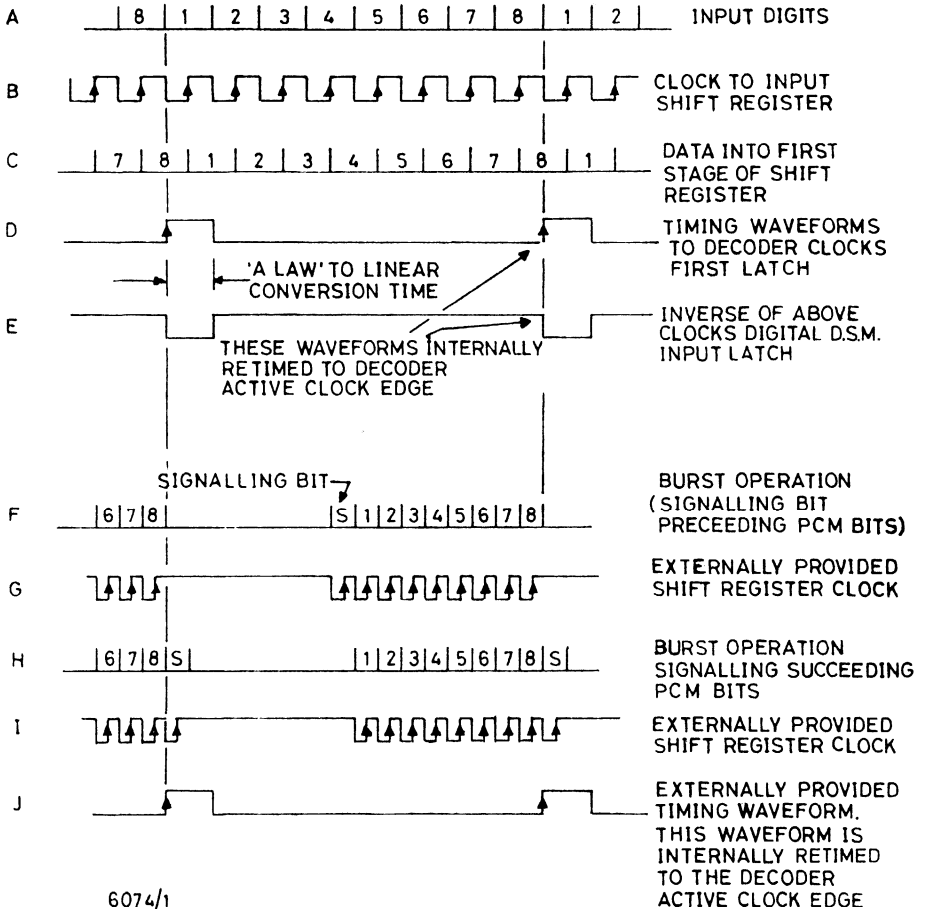
FUNCTIONAL DIAGRAM

6166

131

ZNPCM1

TIMING DIAGRAM
ENCODER

A	TIMING VECTOR
	COUNT VALUE
127 128 255 0 127 128	
B	MOST SIG' BIT OF COUNTER
C	ACCUMULATOR CLEAR
	LINEAR TO 'A LAW' CONVERSION
D	LOAD PULSE TO OUTPUT SHIFT REGISTER
E	64kHz CLOCK TO OUTPUT SHIFT REGISTER
F	SIGN BIT — SHIFT REGISTER OUTPUT
G	64kHz CLOCK TO OUTPUT 'D' TYPE
H	SIGN BIT — 'D' TYPE OUTPUT, SERIAL P.C.M. OUTPUT
I	ZERO SWITCH DELAY
J	ONE BIT DELAY
K	TWO BITS DELAY
L	THREE BITS DELAY
	INTERNALLY GENERATED DECODER TIMING WAVEFORMS (ONLY ONE SELECTED WITH A 2 BIT ADDRESS)
	125 μs
M	EXTERNAL CLOCK TO OUTPUT SHIFT REGISTER
N	SHIFT REGISTER OUTPUT
O	HIGH SPEED CLOCK TO OUTPUT OF 'D' TYPE
P	SERIAL P.C.M. OUTPUT
	TIME FOR OUTPUT OF SIGNALLING BITS

6073/1

132

ZNPCM1

TIMING DIAGRAM
DECODER

A | 8 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 1 | 2 | INPUT DIGITS

B   CLOCK TO INPUT SHIFT REGISTER

C | 7 | 8 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 1 | DATA INTO FIRST STAGE OF SHIFT REGISTER

D   TIMING WAVEFORMS TO DECODER CLOCKS FIRST LATCH

'A LAW' TO LINEAR CONVERSION TIME

E   INVERSE OF ABOVE CLOCKS DIGITAL D.S.M. INPUT LATCH

THESE WAVEFORMS INTERNALLY RETIMED TO DECODER ACTIVE CLOCK EDGE

SIGNALLING BIT

F | 6 | 7 | 8 | | S | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | BURST OPERATION (SIGNALLING BIT PRECEEDING PCM BITS)

G   EXTERNALLY PROVIDED SHIFT REGISTER CLOCK

H | 6 | 7 | 8 | S | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | S | BURST OPERATION SIGNALLING SUCCEEDING PCM BITS

I   EXTERNALLY PROVIDED SHIFT REGISTER CLOCK

J   EXTERNALLY PROVIDED TIMING WAVEFORM. THIS WAVEFORM IS INTERNALLY RETIMED TO THE DECODER ACTIVE CLOCK EDGE

6074/1

133

ZNPCM1

APPLICATIONS INFORMATION

(a) A Single Channel Codec

Fig. 1 shows a block diagram of a single channel Codec using the ZNPCM1. The circuit accepts a band limited analogue input signal (300 – 3,400 kHz) and converts it to one bit/sample delta sigma code format at a high sampling rate. The dsm bit stream is then converted by the ZNPCM1 into 8-bit compressed pulse code modulation (pcm) code words at the standard rate of 8K samples/sec, which is then converted into serial format for transmission serially at 64K bit/sec. External timing signals can be used to increase the transmission bit rate to 2,048K bit/sec. to allow for multiplexing in a burst format (see application b).
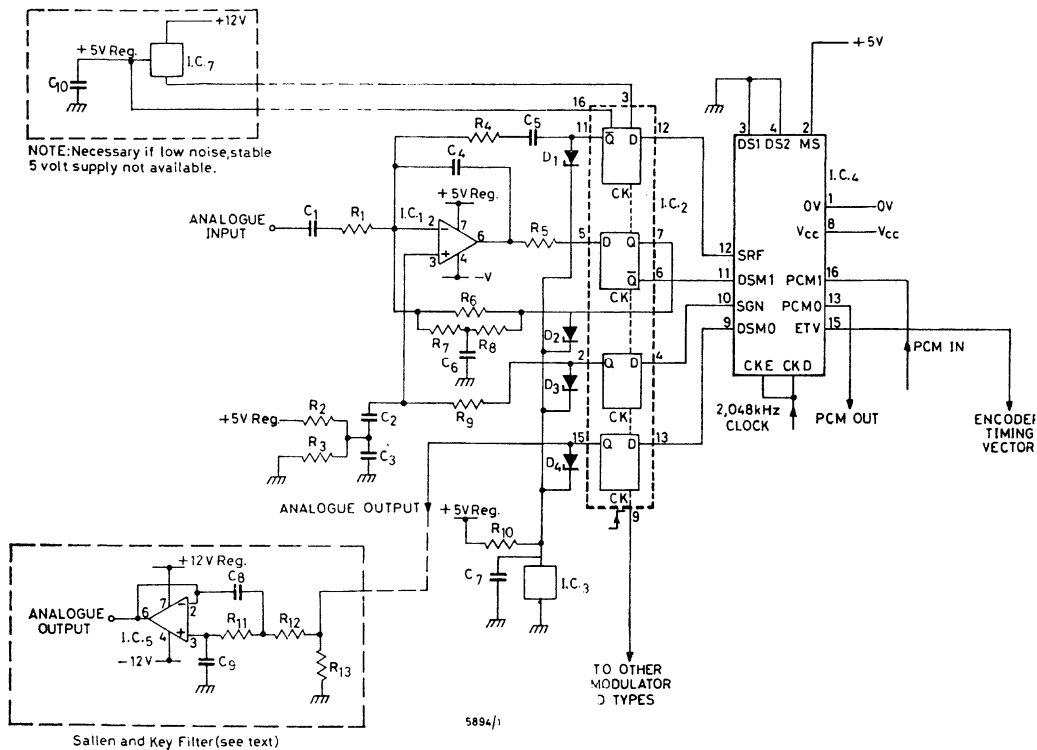
Fig. 1.

The pcm input interface will accept either a 64K bit/sec. bit stream or, by the application of external timing signals, a bit rate of 2,048K bit/sec. in burst format. This is then converted by the ZNPCM1 into a dsm bit stream at 2,048K bit/sec. The dsm demodulator accepts this bit stream and produces one of two precisely defined analogue levels per single bit sample. The analogue waveform can then be recovered via a low pass filter, cutting off just above the highest signal frequency to be recovered (3.4 kHz).

Output voltages of the dsm circuit are stabilised by supplying the quad D-type from a 5 volt regulator, which is always associated with the Codec, and clamping the high state output voltages to a 2.45V reference by the use of Schottky diodes. These also help to match the voltages influencing the d.c. alignment conditions and minimise the effects of power supply variations and noise. Resistor ratio stability is obtained, along with a small modulator/demodulator physical size by implementing the resistors and small capacitors as an in-line hybrid. More details of the operation of the dsm circuit are outlined in the Ferranti brochure 'A Single Channel Codec'.

An interesting development, again in co-operation with the British Post Office, is the integrated circuit dsm solution now approaching completion. This will reduce the circuitry surrounding the ZNPCM1 to a single I.C. and seven capacitors, the latter almost certainly to be made available as a single in-line hybrid.

The Codec performance related to CCITT criteria is outlined in Fig. 2.
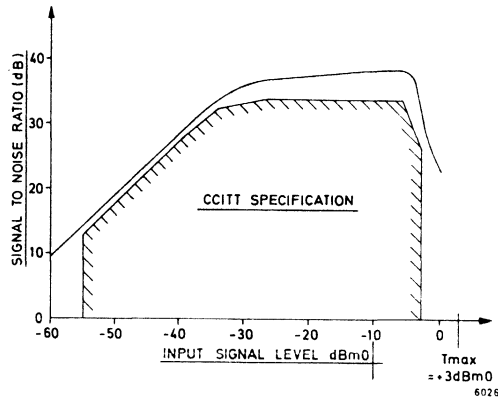
Fig. 2.

(b) A 30 Channel PCM Codec Solution

Traditionally the code conversion process on branch-to-main telephone exchange systems has been performed using multiplexed codecs. Historically the reason for this has been the codec specification where the signal-to-noise and gain-linearity constraints imposed on the systems have resulted in the use of expensive hybrid codecs. It might seem immediately obvious that the use of single channel codecs offers a more attractive solution, however a comparison of one of the major performance criteria is first of all necessary, that of power dissipation. Indeed, an initial comparison using the conventional 30 Channel PCM system shows the single channel codec approach to disadvantage. However, a more detailed analysis, using the single channel codecs in a power switching mode, shows this technique to be compatible with time shared codecs. This is described in section (d).

Let us first of all consider the system approach for using the single channel codecs in a 30 Channle PCM system by looking at Fig. 3.

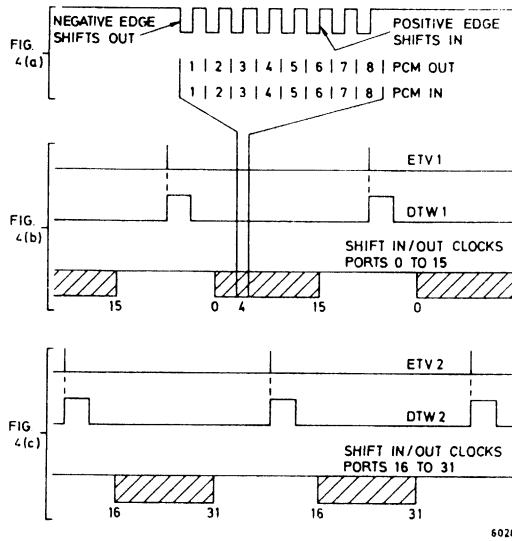# ZNPCM1

i = 1 FOR 0 < N ≤ 15
i = 2 FOR 16 < N ≤ 31
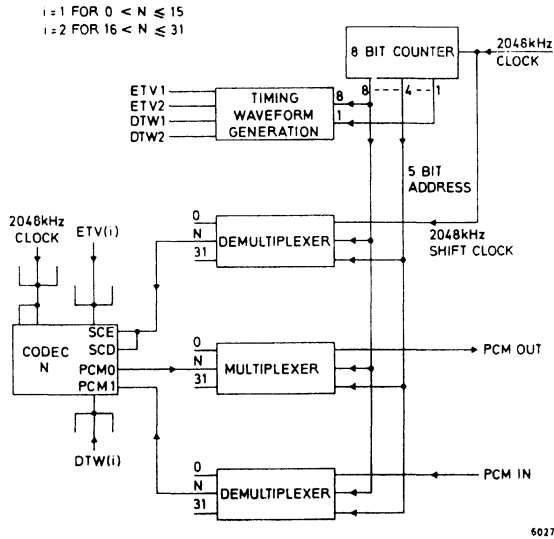
Fig. 3.

Fig. 3 shows how a 32 time slot (Note: A 30 Channel system has in fact, 32 time slots, the two additional ones being for signalling notation and synchronisation), 2,048K bit/sec. multiplex can be formed and decoded using 30 single channel codecs, when the two directions of transmission operate synchronously. Only the Nth codec is shown, connected to the 'Nth' port of the 32 port multiplexer and demultiplexers. When the 5-bit address equals N the 2,048 kHz shift clock is routed through the 'Nth' codec for eight clock pulses as shown in Fig. 4(a). The shift-in and shift-out clock terminals of the codec are commoned together. Since the shift-out terminal uses a negative active clock edge and the shift-in terminal uses a positive active clock edge the pcm digits for the two directions may be in exact time alignment. This is compatible with using the same 5-bit address for the multiplexer and the other demultiplexer.

The Encoder Timing Vector (ETV) and the Decoder Timing Waveform (DTW) may be derived from a counter driven by the 2,048 kHz clock and commoned across a number of codecs. For a 32 time slot multiplex, two sets of ETV's and DTW's should be generated with a half frame displacement as shown in Figs. 4(b) and 4(c). The first pair will supply ports 0 to 15 and the second pair ports 16 to 31, and consequently allowing the shift activity to be kept well clear of the timing waveforms for a given codec.

For a conventional 32 time slot codec ports 0 and 16 correspond to the synchronisation and signalling channels respectively.

Fig. 5 shows a similar arrangement for generating and decoding a 32 time slot multiplex when the two directions of transmission operate asynchronously. The two directions are operated quite independently but using similar principals to those previously discussed. It should again be noted that two sets of ETV's and DTW's should be used.

Fig. 4.

Fig. 5.

137
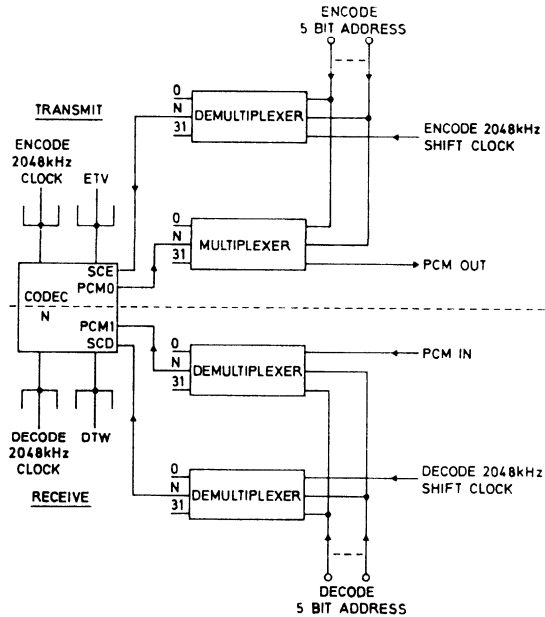
ZNPCM1

(c) Switching Applications

The ZNPCM1 can be used in a variety of ways to satisfy switching applications. One technique is to operate directly on the 2,048K bit/s digit stream produced by the circuit arrangement shown in Fig. 3, where each codec has a defined time slot in the bit stream. An alternative technique would be to derive the address applied to the multiplexer and demultiplexer from the contents of a random access memory (RAM) which defines the codec to be used in a given time slot, in an exchange of PCM codewords between the codec and an intermediate store. In this mode of use the codec interface is effectively used as a time switch store.

The circuit shown in Fig 5 can be used without an intermediate store where again the codec addresses are derived from RAM's. The encode address defines the 'source' and the decode address the 'sink' in a given time slot. The decode address may be delayed with respect to the encode address by an integer number of 2,048 kHz clock periods to take account of any small, fixed switching delay.
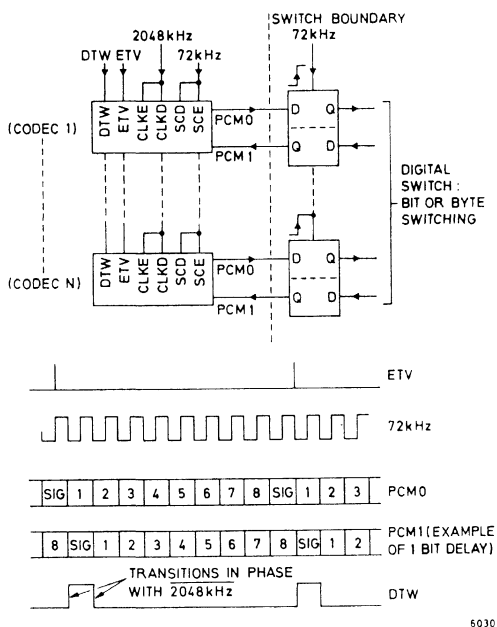
Fig. 6.

Fig. 6 shows an arrangement where the codecs input and output continuously, allowing 9-bits (8 PCM plus 1 signalling) to be exchanged in each 125 µs sample period. All the codecs may be supplied with common ETV, DTW, 2,048 kHz and 72 kHz waveforms. Each bit is retimed in the digital switch using a latch.

The digital switch may be operated using a bit switching arrangement, combined with the extraction and insertion of the signalling bits. Alternatively the bits may be reformatted into bytes and then byte switching performed. If the signalling is handled separately to the pcm codewords then a 64K bit/s rate can be used to and from the codec. This is compatible with using the codecs internal clock mode (MS = 1) in which case the only common timing waveforms required at the codec are the 2,048 kHz clock and the ETV.

138

(d) Power Switching

Comparisons have previously been made between shared and single channel codecs where these comparisions were reduced to one of power dissipation. Considerable power savings can be made by using the codecs in such a mode that they are only powered-up when required for use.

It is interesting to compare the power dissipation of an eight channel system using in one case eight ZNPCM1s in a power switching mode and, in the other case, one of the more popular time shared codecs which caters for eight channels. One single channel codec dissipates 600 mW and the time shared codec dissipates 1500 mW.

If the channel occupancy is p, then the average power dissipation per channel for the time shared codec is given by

$$W_{TS} = 1 - (1-p)^8 \frac{1500}{8} \, mW$$

This assumes the time shared codec is only powered-up when any of the eight channels are required for use.

The average power dissipation per channel using the single channel codecs is simply given by,

$$W_{SC} = p.600 \, mW$$

Fig. 7 shows a plot of power dissipation versus channel occupancy ; p for both approaches. The busy period average channel occupancies are likely to be in the range 0.2 to 0.15, clearly the lower end of the curves. Taking a figure of p = 0.06, for example, then the single channel codec dissipates only 36 mW per channel, approximately 50% less than the time shared codec. As the graph shows even for very busy exchanges given values for p of up to 0.3 shows the ZNPCM1 system to dissipate less power.
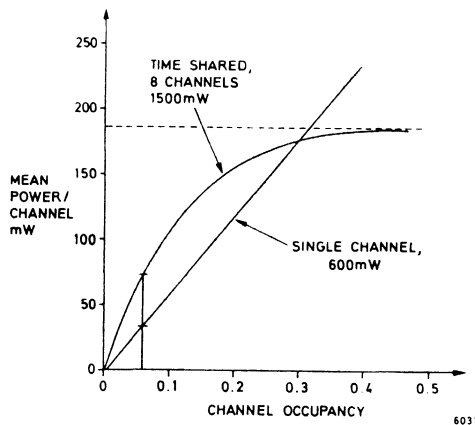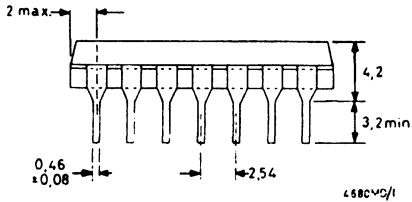

Fig. 7.

ZNPCM1

PIN CONNECTIONS

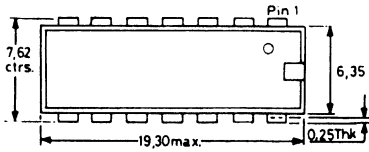|			
0V	1	24	I.C.
MS	2	23.	N C.
DS1	3	22	SCD
DS2	4	21	CLK E
ADI	5	20	CLK D
N.C.	6	19	SCE
0V	7	18	DTW
V_{cc}	8	17	SGBO
DSMO	9	16	PCMI
SGN	10	15	ETV
DSMI	11	14	SGBI
SRF	12	13	PCMO

6234/1

CHIP DIMENSIONS AND LAYOUT

163 MIL

V_{CC} GND   AD1 DS2

DSMO —   — DS1
SGN —   — MS
DSM1 —   — GND
SRF —
PCMO —
SGB1 —   — SCD
ETV —

179 MIL

PCMI   SGBO   DTW   SCE   CLK D   CLK E

6237
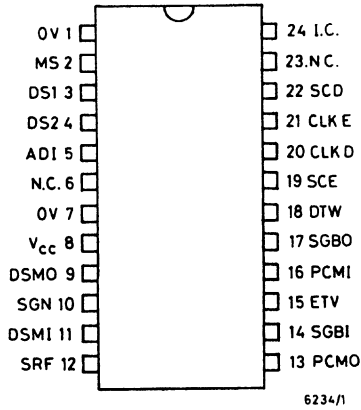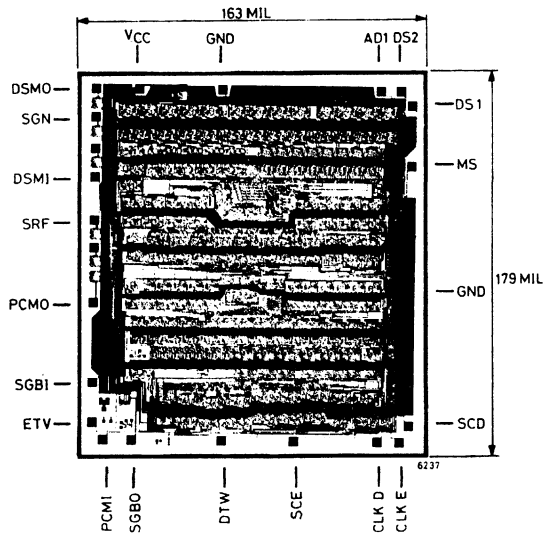
8. PACKAGE DETAILS

ZN426E-8 ZN429E-8
ZN426E-7 ZN429E-7
ZN426E-6 ZN429E-6

ZN426J-8
ZN429J-8

14 Lead Moulded D.I.L.
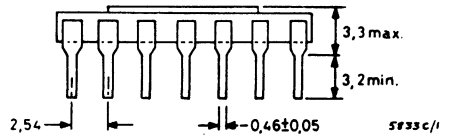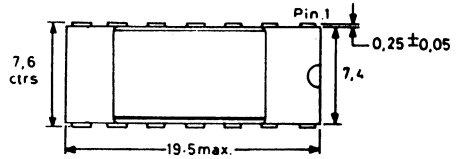
14 Lead Ceramic D.I.L.

ZN425E-8
ZN425E-7
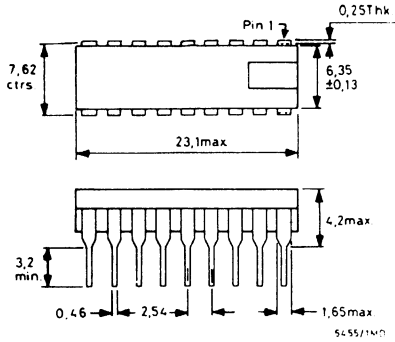ZN425E-6
ZN428E-8
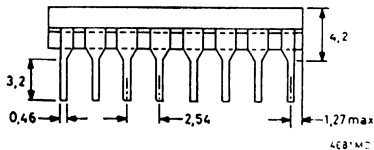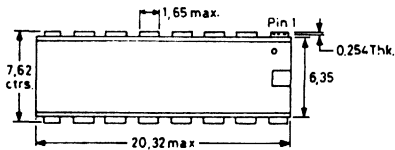
ZN425J
ZN428J-8

16 Lead Moulded D.I.L.
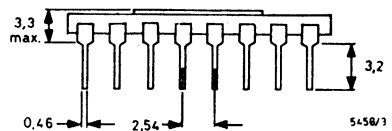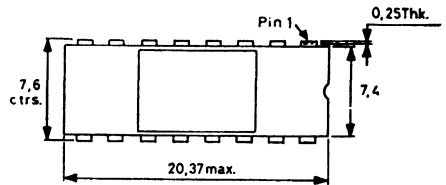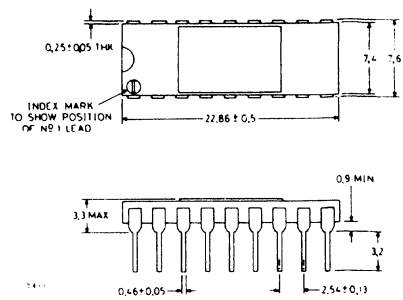
16 Lead Ceramic D.I.L.

Dimensions in millimetres
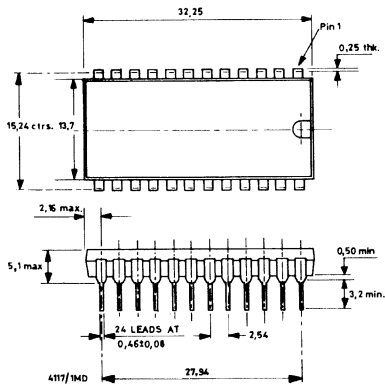
141

ZN427E-8

18 Lead Moulded D.I.L.

ZN427J-8

18 Lead Ceramic D.I.L.

ZNA116E
ZNPCM1E

ZNPCM1J
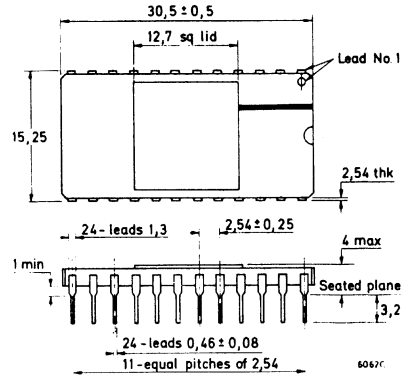
24 Lead Ceramic D.I.L.

Dimensions in millimetres
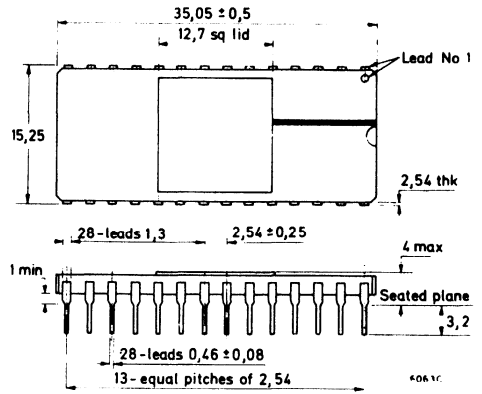
ZNA216E

37,4 Max.

0,25 thk.

15,25

Indent - Pin 1

2,16 Max

5,1 Max

0,50 Min.

3,2 Min

28 leads - 0,46 ± 0,08

13 equal pitches of 2,54

4116MD/2
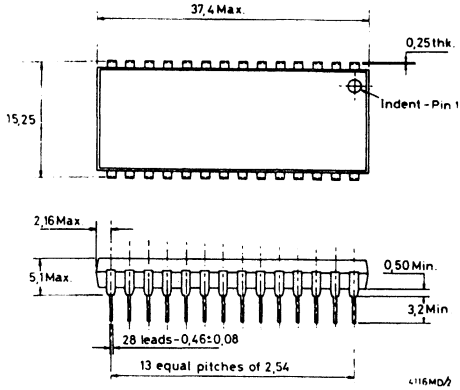
28 Lead Moulded D.I.L.
SO-119E

ZN432
ZN433
ZNA216J

35,05 ± 0,5

12,7 sq lid

Lead No 1

15,25

2,54 thk

28 - leads 1,3

2,54 ± 0,25

4 max

1 min

Seated plane

3,2

28 - leads 0,46 ± 0,08

13 - equal pitches of 2,54

606 3C

28 Lead Ceramic D.I.L.
SO-119E

Dimensions in millimetres